CL74AUP1G02 Low Power Single 2-Input Positive NOR-Gate

General Description

This single 2-input positive-NOR gate is designed for 0.8-V to 3.6-V VCC operation.

The CL74AUP1G02 performs the Boolean function $Y = \overline{A + B}$ in positive logic

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

The CL74AUP1G02 device is available in a variety of packages, including SOT23-5S, C70.

Ordering Information

Part Number	Marking	Package
CL74AUP1G02_235	P02XW	SOT-23-5
CL74AUP1G02_70	PBXW	SC70

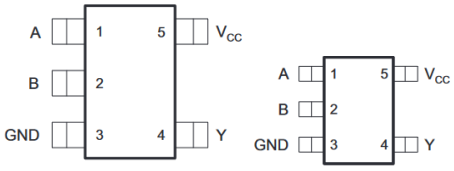
Features

- Inputs Accept Voltages 0.8V to 3.6 V
- Max Tpd of 5 ns at 3.3 V
- Low Static-Consumption, 0.9-μA Max I_{CC}
- Low Noise Overshoot and Undershoot<10% of V_{CC}
- Ioff Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input(V_{hys}= 250mV Typical 3.3V)
- 3.6V I/O Tolerant to Support Mixed-Mode Signal Operation
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

Applications

- ATCA Solutions
- Active Noise Cancellation (ANC)
- Barcode Scanner
- Blood Pressure Monitor
- CPAP Machine
- Cable Solutions
- DLP 3DMachine Vision, Hyperspectral Imaging, Optical Networking, and Spectroscopy
- E-Book
- Embedded PC
- Field Transmitter: Temperature or Pressure Sensor
- Fingerprint Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning

Pin Configuration



Simplified Schematic

Pin Assignment

Pin Name	Pin No.	Pin Function
A	1	Input
B	2	Input
GND	3	Ground
Y	4	Output
VCC	5	Power pin

Absolute Maximum Ratings (Note1)

- V_{CC} ---------- -0.5V to +4.6V
- V_I ---------- -0.5V to +4.6V
- V_O (Voltage range applied to any output in the high-impedance or power-off state) ---------- -0.3V to +4.6V
- V_O (Voltage range applied to any output in the high or slow state) ---------- -0.3V to V_{CC}+0.3V
- Input clamp current ---------- -50mA
- Output clamp current ---------- -50mA
- Continuous clamp current ---------- ±20mA
- Storage Temperature ---------- –65°C to 150°C

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{CC}	Operating	0.8		3.6	V
Input voltage	V_I		0		3.6	V
Output voltage	V_O		0		VCC	V
High- level input voltage	V_{IH}	V_{CC} = 0.8V	V_{CC}			V
		V_{CC} = 1.1V to 1.95V	0.65 xV_{CC}			
		V_{CC} = 2.3V to 2.7V	1.6			
		V_{CC} = 3V to 3.6V	2			
Low- level input voltage	V_{IL}	V_{CC} = 0.8V			0	V
		V_{CC} = 1.1V to 1.95V			0.35 x V_{CC}	
		V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 3V to 3.6V			0.9	

High- level output current	I_{OH}	V_{CC} = 0.8V			-20	uA
		V_{CC} = 1.1V			-1.1	mA
		V_{CC} = 1.4V			-1.7	
		V_{CC} = 1.65V			-1.9	
		V_{CC} = 2.3V			-3.1	
		V_{CC} = 3V			-4	
Low- level output current	I_{OL}	V_{CC} = 0.8V			20	uA
		V_{CC} = 1.1V			1.1	mA
		V_{CC} = 1.4V			1.7	
		V_{CC} = 1.65V			1.9	
		V_{CC} = 2.3V			3.1	
		V_{CC} = 3V			4	
Input transition rise or fall rate	△T/△V	V_{CC} = 0.8V to 3.6V			200	ns/V
Operating temperature	T_A		-40		85	℃

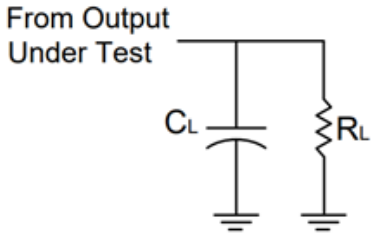
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
High- level output voltage	V_{OH}	V_{CC} = 0.8~3.6V, I_{OH}= -20uA	V_{CC}-0.1			V
		V_{CC} = 1.1V, I_{OH}= -1.1mA	0.75 xV_{CC}			
		V_{CC} = 1.4V, I_{OH}= -1.7mA	1.11			
		V_{CC} = 1.65V, I_{OH}= -1.9mA	1.32			
		V_{CC} = 2.3V, I_{OH}= -2.3mA	2.05			
		V_{CC} = 2.3V, I_{OH}= -3.1mA	1.9			
		V_{CC} = 3V, I_{OH}= -2.7mA	2.72			
		V_{CC} = 3V, I_{OH}= -4mA	2.6			
Low- level output voltage	V_{OL}	V_{CC} = 0.8~3.6V, I_{OL}= 20uA			0.1	V
		V_{CC} = 1.1V, I_{OL}= 1.1mA			0.3 xV_{CC}	
		V_{CC} = 1.4V, I_{OL}= 1.7mA			0.31	
		V_{CC} = 1.65V, I_{OL}= 1.9mA			0.31	
		V_{CC} = 2.3V, I_{OL}= 2.3mA			0.31	
		V_{CC} = 2.3V, I_{OL}= 3.1mA			0.44	
		V_{CC} = 3V, I_{OL}= 2.7mA			0.31	
		V_{CC} = 3V, I_{OL}= 4mA			0.44	
Input leakage current	I_I	V_{IN}= 3.6V or GND, V_{CC}= 0~3.6V			0.1	uA
Power off leakage current	I_{OFF}	V_I or V_O=0V to 3.6V, V_{CC}=0V			0.2	uA
Supply current	I_{CC}	V_I= GND or (V_{CC} to 3.6V), I_{OUT}=0, V_{CC}=0.8~3.6V			0.5	uA
Additional supply current per input pin	△I_{CC}	V_I= V_{CC}-0.6V, I_{OUT}=0			40	uA

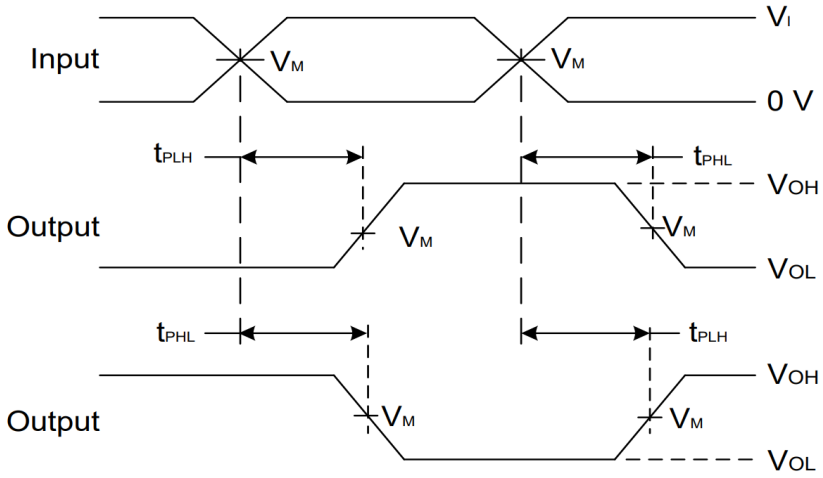
Switching Characteristics

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
Propagation delay from input(A or B) to output(Y)	T_{PD}	V_{CC} = 0.8V	C_L=15pF R_L=1MΩ		25		ns
		V_{CC} = 1.2V±0.1V,		3.6	9.9	16.5	
		V_{CC} = 1.5V±0.1V,		2.3	7.2	11.3	
		V_{CC} = 1.8V±0.15V		1.6	5.8	8.9	
		V_{CC} = 2.5V±0.2V		1	4.3	6.1	
		V_{CC} = 3.3V±0.3V		1	3.4	5	

Parameter Measurement Information



VCC	INPUTS		VM	CL	RL
	VI	tr/tf			
0.8V	VCC	≦2ns	VCC/2	15pF	1MΩ
1.2V ± 0.1V	VCC	≦2ns	VCC/2	15pF	1MΩ
1.5V ± 0.1V	VCC	≦2ns	VCC/2	15pF	1MΩ
1.8V ± 0.15V	VCC	≦2ns	VCC/2	15pF	1MΩ
2.5V ± 0.2V	3V	≦2.5ns	1.5V	15pF	1MΩ
3.3V ± 0.3V	VCC	≦2.5ns	VCC/2	15pF	1MΩ



Voltage Waveform Propagation Delay Times
Inverting and Non Inverting Outputs

Notes: A. C_L includes probe and jig capacitance
B. All pulses and supplied at pulse repetition rate≦10MHz
C. The Inputs are measured separately one transition per measurement
D. t_{PLH} and t_{PHL} are the same as t_{PD}

IC Operation Information

Basic Operation

The CL74LVC1G02 device contains one 2-input positive NOR gate device and performs the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \bullet \overline{B}$. The AUP family of devices has quiescent power consumption less than 1 µA. This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered. The Ioff feature also allows for live insertion.

Function Block Diagram

Feature Description

- Wide operating Vcc range of 0.8V to 3.6V.
- 3.6-V I/O tolerant to support down translation.
- Input hysteresis allows slow input transition and better switching noise immunity at the input.
- Ioff feature allows voltages on the inputs and outputs when V_{CC} is 0 V.
- Low noise due to slower edge rates.

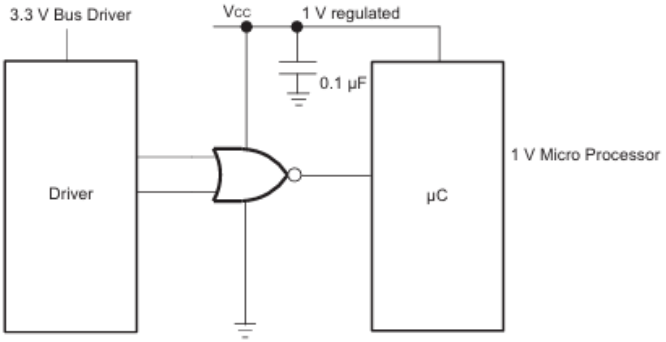
Device Functional Table

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

IC Application Information

The AUP family is the solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire VCC range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

Typical Application



Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits

Detailed Design Procedure

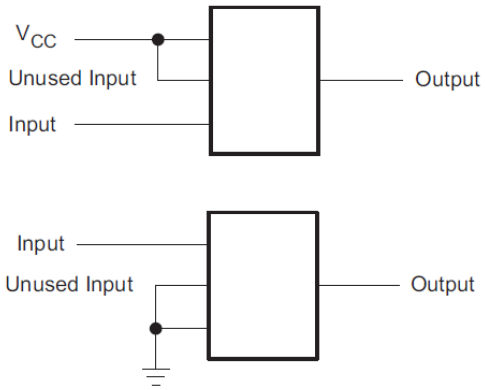
1. Recommended Input conditions:
   – Rise time and fall time specs. See (Δt/ΔV)
   – Specified high and low levels. See (VIH and VIL)
   – Inputs are overvoltage tolerant allowing them to go as high as 3.6 V at any valid VCC
2. Recommended output conditions:
   – Load currents should not exceed 20 mA on the output and 50 mA total for the part
   – Outputs should not be pulled above VCC

Power Supply Recommendations

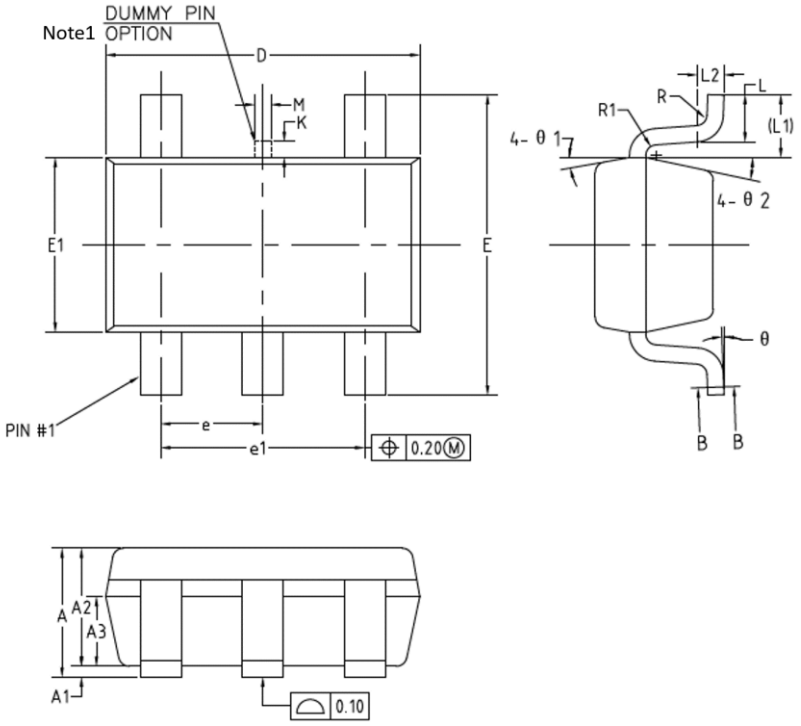
The power supply can be any voltage between the Min and Max supply voltage rating located in the Recommended Operating Conditions table. Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended; if there are multiple VCC pins, then 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and a 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

Layout Considerations

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Below figure specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.



Package Information
SOT23-5

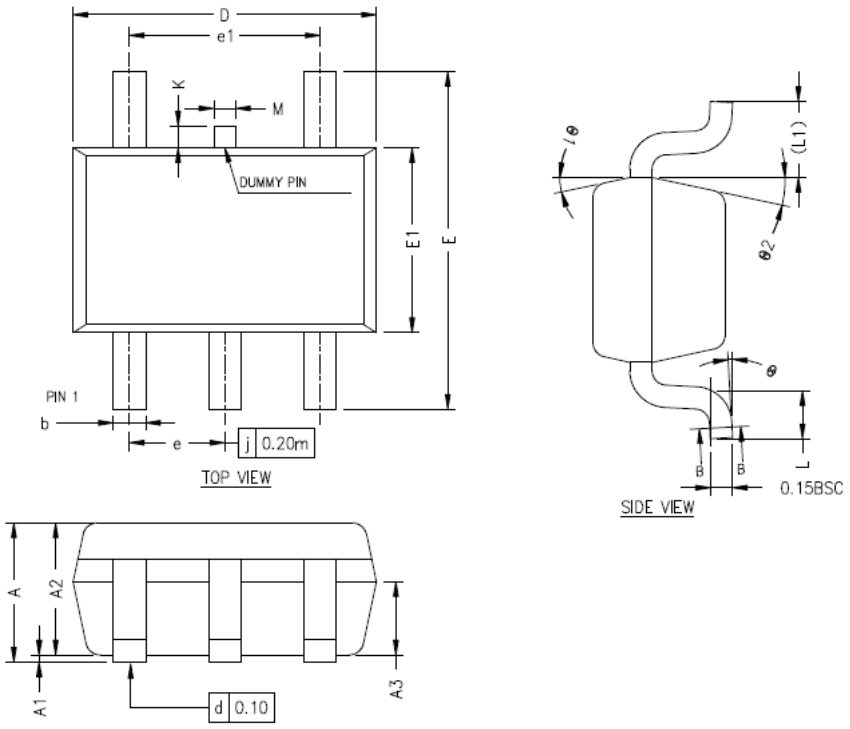


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

	SYMBOL	MIN	NOM	MAX
	A	–	–	1.25
	A1	0	–	0.15
	A2	1.00	1.10	1.20
	A3	0.60	0.65	0.70
4	b	0.34	–	0.45
4	b1	0.34	0.38	0.41
4	c	0.12	–	0.20
4	c1	0.12	0.15	0.16
	D	2.826	2.926	3.026
	E	2.60	2.80	3.00
3	E1	1.526	1.626	1.700
	e	0.90	0.95	1.00
	e1	1.80	1.90	2.00
2	K	0	–	0.20
	L	0.30	0.40	0.60
	L1		0.59REF	
	L2		0.25BSC	
2	M	0.10	0.15	0.20
	R	0.05	–	0.20
	R1	0.05	–	0.20
	θ	0°	–	8°
	θ 1	8°	10°	12°
	θ 2	10°	12°	14°

Notes: 1. Dummy pin may differ or may not be present.

Package Information
SC70



COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	–	1.10
A1	0	–	0.10
A2	0.80	0.90	1.00
A3	0.40	0.50	0.60
b	0.17	–	0.30
b1	0.17	0.22	0.25
3 c	0.12	–	0.20
3 c1	0.12	0.15	0.16
D	2.02	2.07	2.12
E	2.20	2.30	2.40
E1	1.21	1.26	1.31
e	0.60	0.65	0.70
e1	1.20	1.30	1.40
L	0.26	0.33	0.46
L1		0.52REF	
2 M	0.10	0.15	0.20
2 K	0	–	0.20
θ	0°	–	8°
θ1	10°	12°	14°
θ2	10°	12°	14°