Chip1 Product Overview

Chip1 Martin Tseng

Outline

- IC 基礎概論
  - Power IC • Logic IC • Load Switch
- LDO 規格書介紹
- LDO 選擇原則

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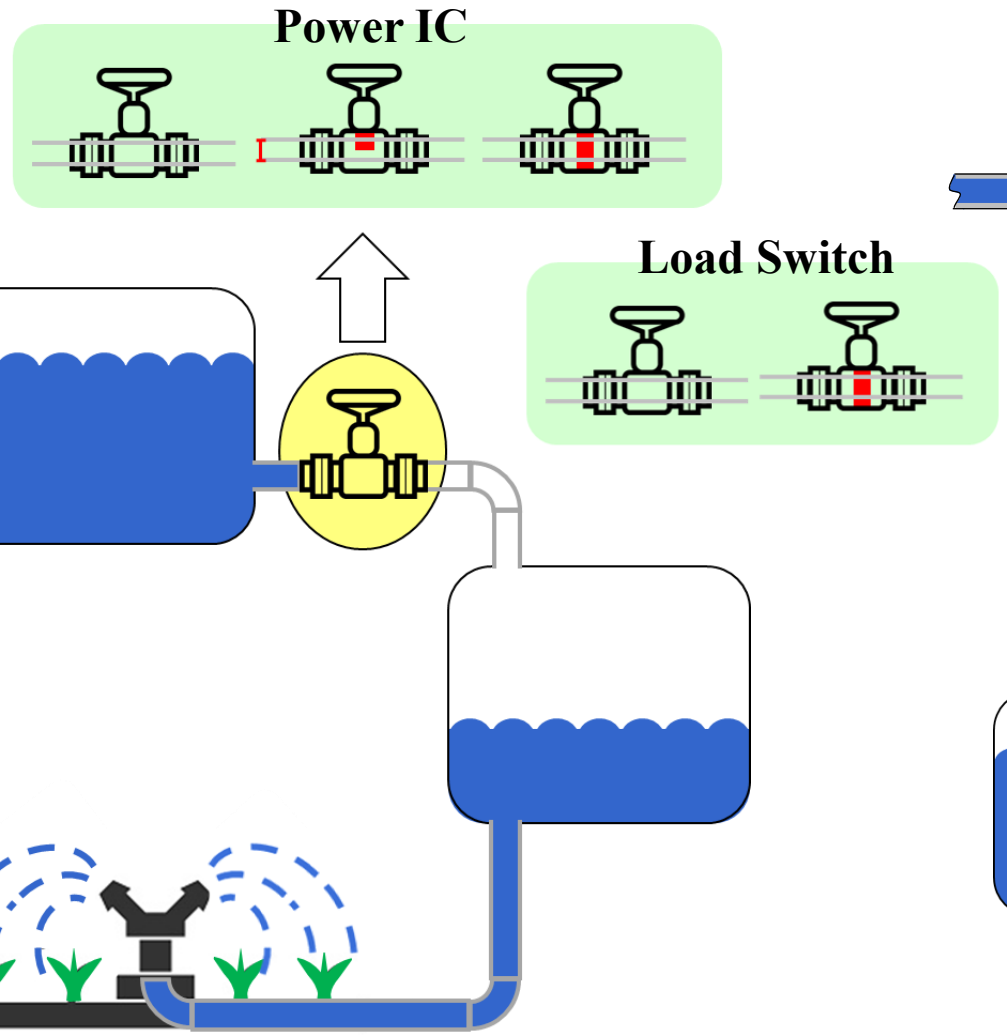
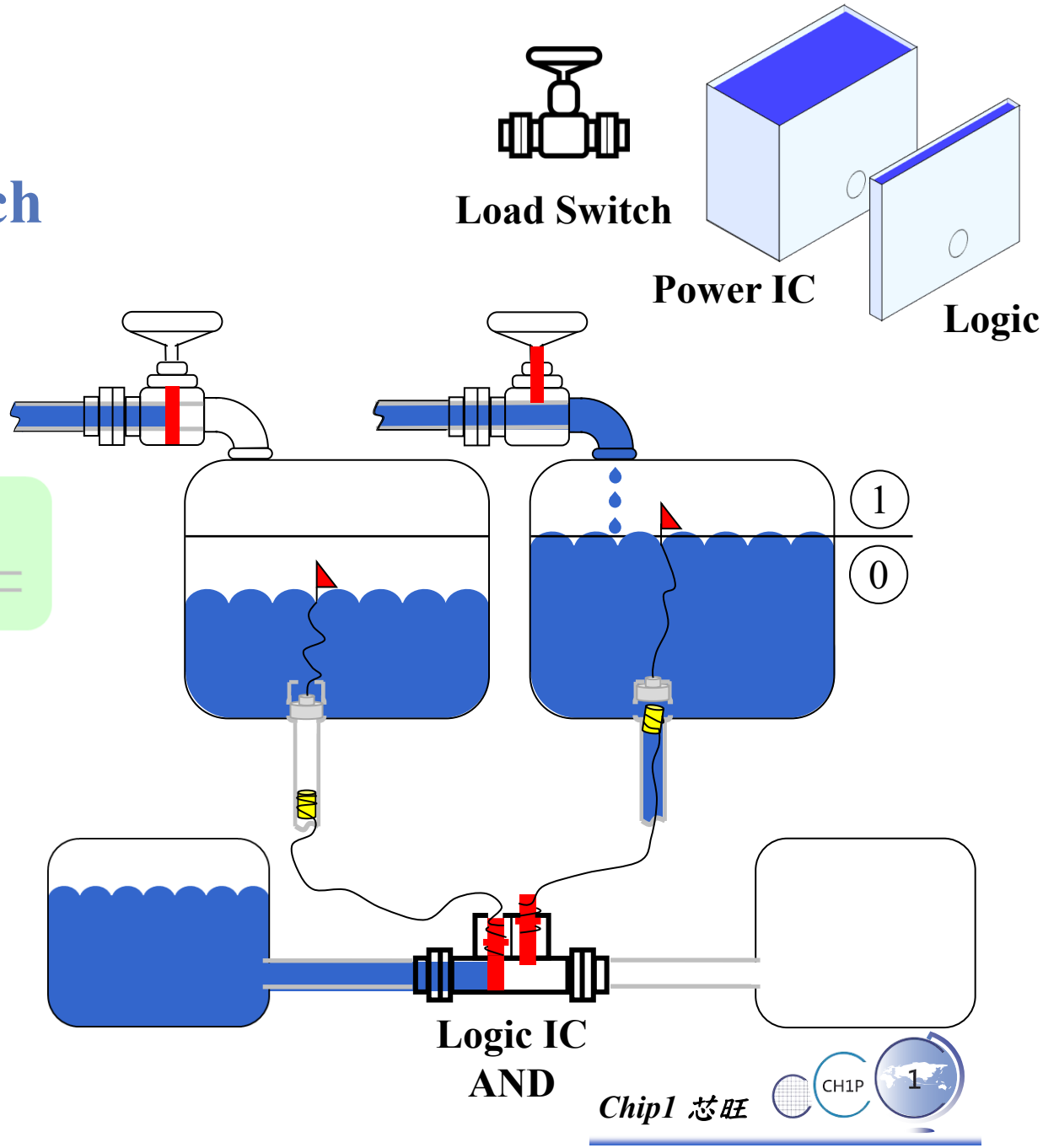
IC 基礎概論

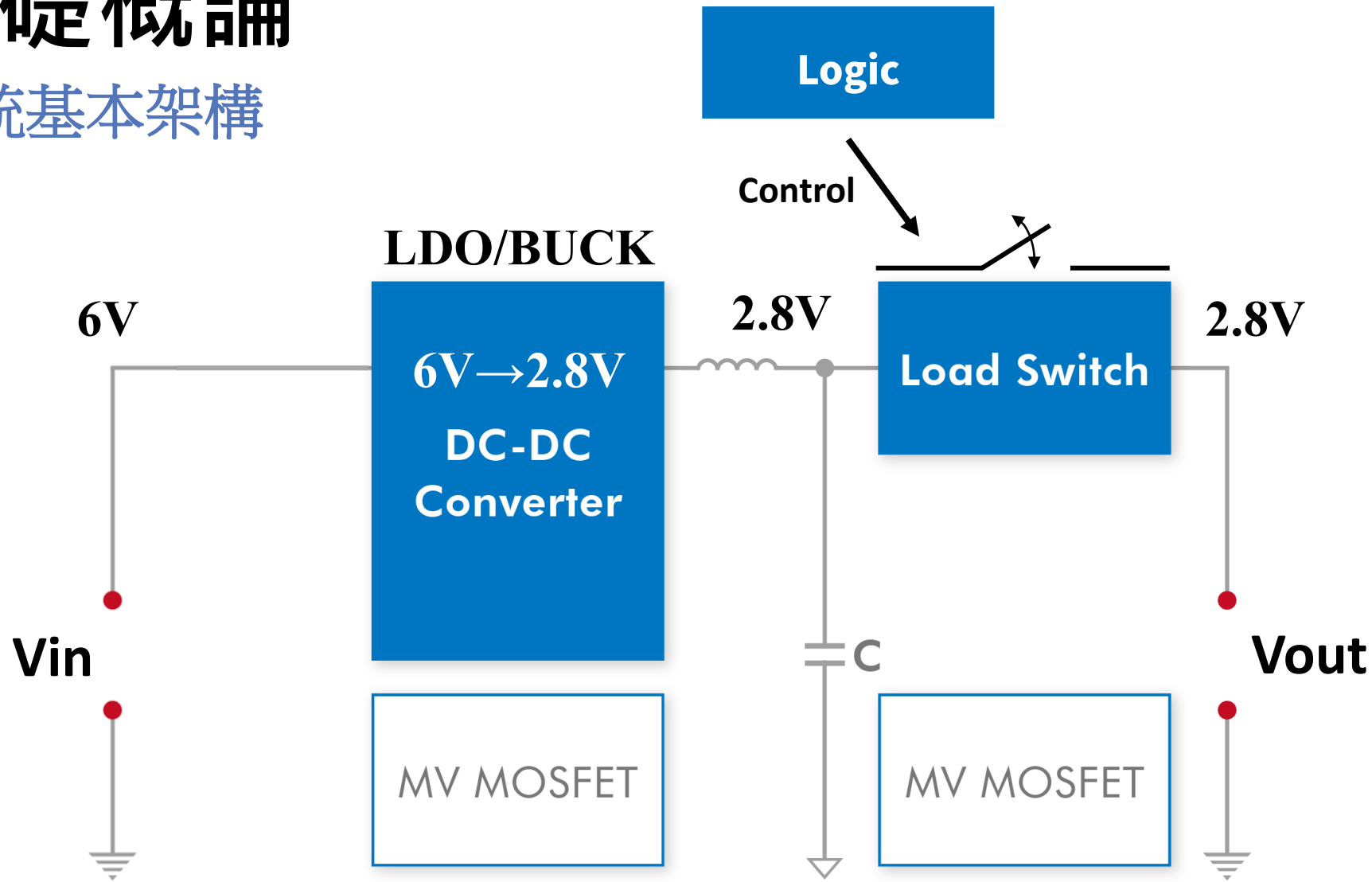
Power IC • Logic IC • Load Switch





IC 基礎概論

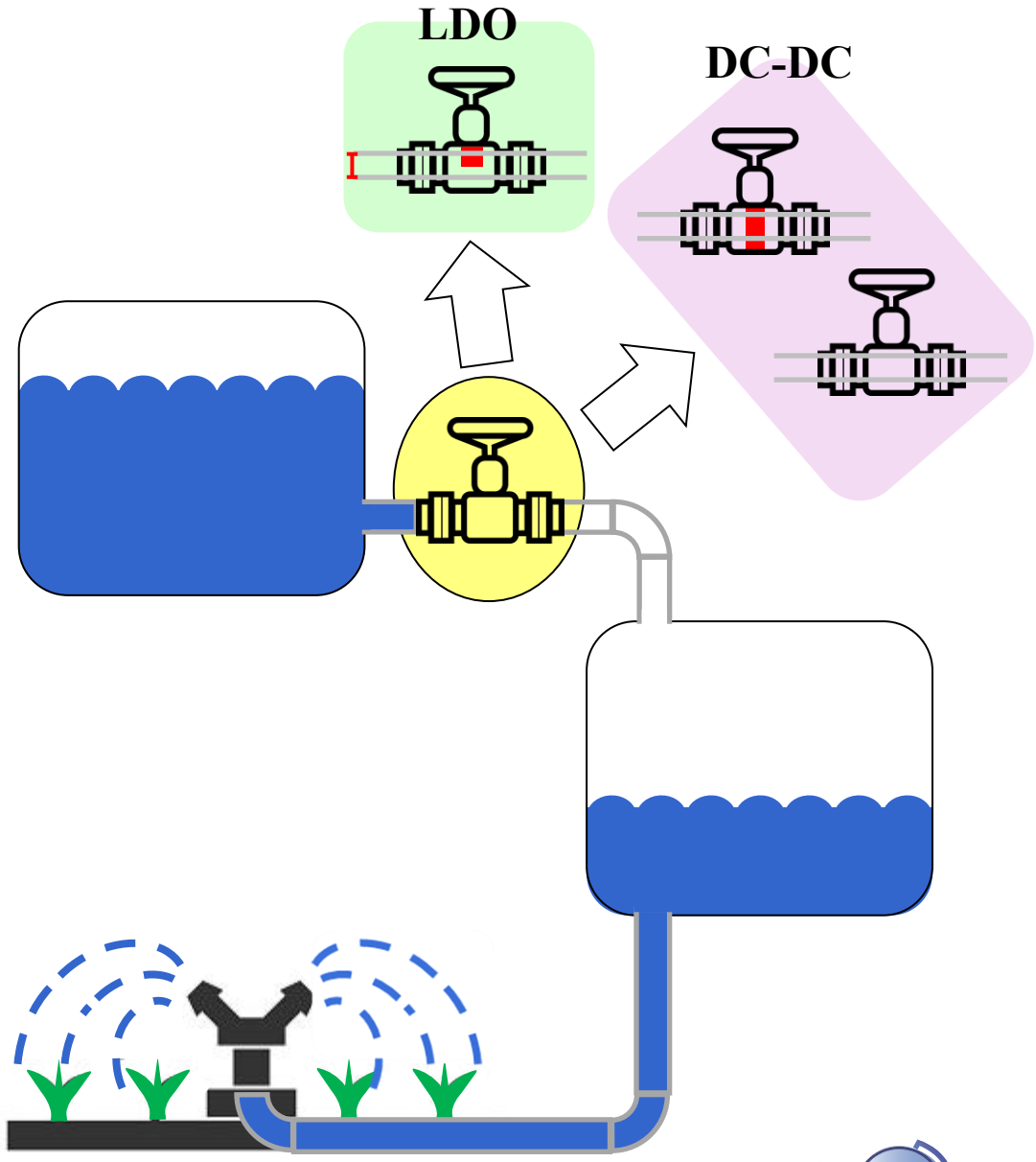
電子系統基本架構



IC 基礎概論

Power IC

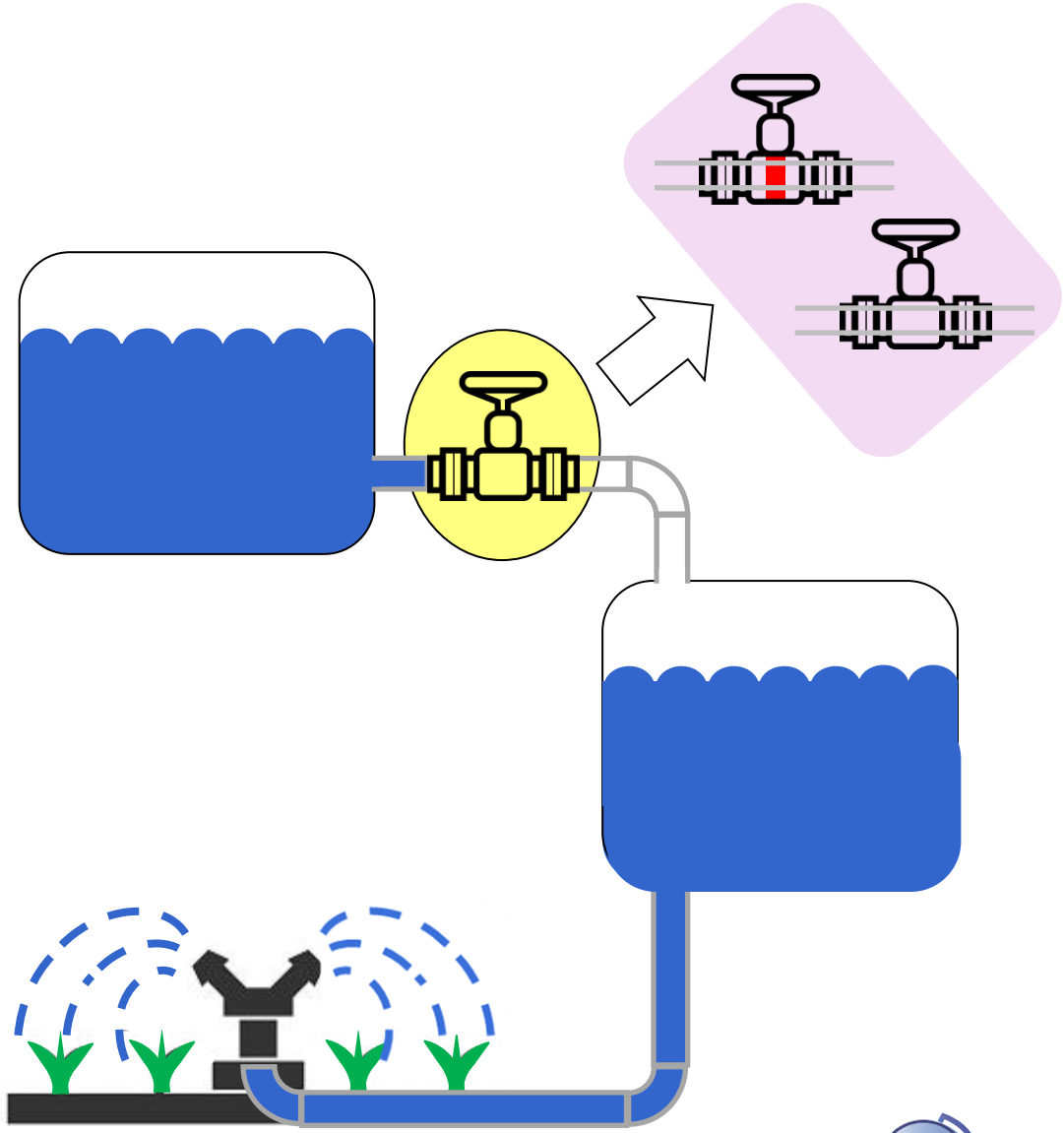
LDO	DC-DC (Buck , Boost Converter)
低壓差、小電流應用	高壓差、大電流應用
僅能降壓	可降壓、升壓與升降壓 ✓
雜訊較低 ✓	雜訊相對較高
效率較低	效率較高 ✓
壓差大時容易發熱	散熱表現較佳 ✓
電路單純、成本較低 ✓	電路複雜、成本較高
靜態功耗較低 ✓	靜態功耗相對較高



IC 基礎概論

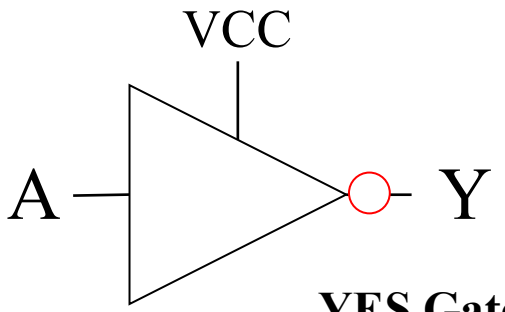
Load Switch

Load Switch	MOSFET
整合式電源控制 IC	**離散式開關元件**
具有保護功能 OCP/OTP/UVLO	無內建保護
Gate 驅動 內建Gate Driver / Charge Pump	Gate 驅動 需外部驅動電路
具有緩啟動	無緩啟動 需額外電路實現
電路整體系統較簡化	外部設計較多
緩啟動降低 導通產生Inrush Current	外部電路降低 導通產生Inrush Current



IC 基礎概論

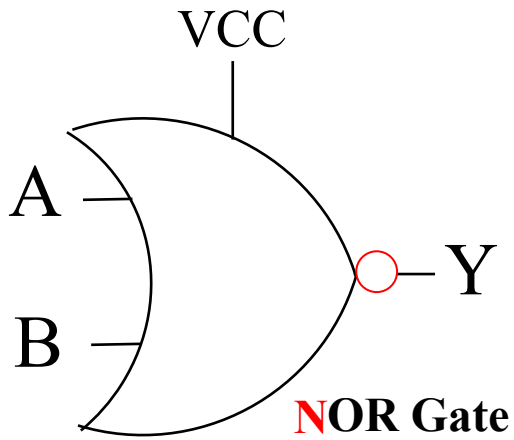
Logic IC



YES Gate

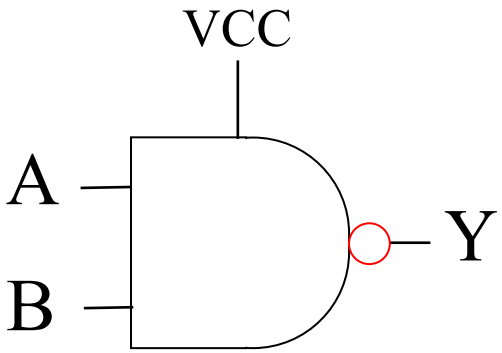
NOT Gate

Input	Output	Output
A	Y	Y
0	0	1
1	1	0



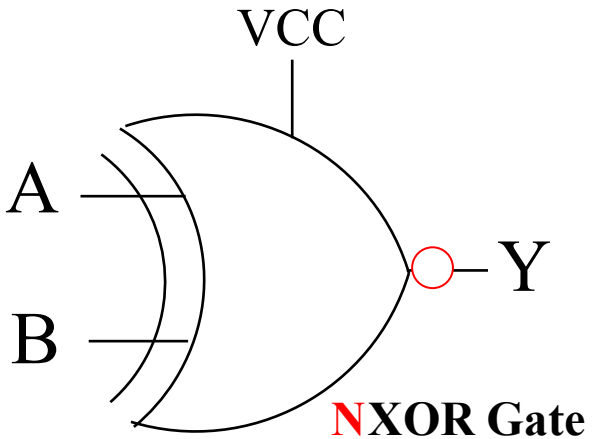
NOR Gate

Input		Output	Output
A	B	Y	Y
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0



NAND Gate

Input		Output	Output
A	B	Y	Y
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0



NXOR Gate

Input		Output	Output
A	B	Y	Y
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

IC 基礎概論

Logic IC 產品

1/2/3/4/6 Channel	1/2/3/4/6 Channel	1/4 Channel	1/4 Channel
CL74LVC1G/2G/3G/XXA	CL74AUP1G/2G/3G/XXA	CL74LV1T/XXA	CL74AUP1T/XXA
SOT23 / SC70 / SOP / TSSOP Input=1.65V->5.5V	SOT23 / SC70 / SOP / TSSOP Input=0.8V->3.6V	SOT23 / SC70 Input=1.5V->5.0V	SOT23 / SC70 Input=2.3V->3.6V
Buffer/Inverter	Buffer/Inverter	Buffer/Inverter	Buffer/Inverter
3-State Schmitt-Trigger Open-Drain	3-State Schmitt-Trigger Open-Drain	3-State Schmitt-Trigger	3-State Schmitt-Trigger
AND/NAND	AND/NAND	AND/NAND	AND/NAND
OR/NOR	OR/NOR	OR/NOR	OR/NOR
XOR/XNOR	XOR/XNOR	XOR/XNOR	XOR/XNOR

Outline

- IC 基礎概論
  - Power IC • Logic IC • Load Switch
- **LDO 規格書介紹**
- LDO 選擇原則

LDO 規格書介紹

概述（General Description)

提供IC的基本功能以及特性整體描述

訂購資訊(Ordering Information)

產品料耗、封裝和電壓版本等資訊

特性(Features)

IC主要功能和優點，如低功耗、低壓差等。

應用(Applications)

說明IC適合的產品，如手機、白色家電等。

引腳配置(Pin Configuration)

IC各封裝引腳排列示意圖

典型應用電路(Typical Application Circuit)

IC實際在應用中參考電路圖配置

CHIP 1

CR2503

500nA I_Q, 300mA Low-Dropout Linear Regulator

General Description

The CR2503 ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. With less than 500nA quiescent current at no load, the CR2503 is ideally suited for standby micro-control-unit systems, especially for always-on applications like portable, and other battery-operated systems. The CR2503 retains all the features that are common to low dropout regulators including a low dropout PMOS pass device, short circuit protection, and thermal shutdown.

The CR2503 has a 6V maximum operating voltage limit, a -40°C to 125°C junction operating temperature range, and ±2% output voltage tolerance. The CR2503 is available in SOT23-3, SOT23-5, and DFN1X1 surface mount packages.

Ordering Information

Part Number	Package	XXX: Voltage
CR2503_XXX_233A	SOT23-3	12 : 1.2V 15 : 1.5V 18 : 1.8V 25 : 2.5V 28: 2.8V 33 : 3.3V
CR2503_XXX_235	SOT23-5	
CR2503_XXX_1014	DFN1X1-4L	
CR2503_XXX_1516	DFN1.5X1.5-6	

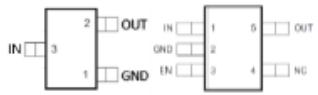
Features

- V_{IN} Range up to 6V
- Output Voltage Tolerances of ±2%
- Output Current of 300mA
- Ultra Low Quiescent Current (I_Q = 500nA)
- Dropout Voltage Typically 500mV at I_{OUT} = 300mA
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limit
- Ceramic Capacitor Stable

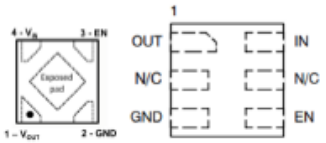
Applications

- Portable, Battery Powered Equipment
- Ultra Low Power Microcontroller
- Notebook computers

Pin Configuration

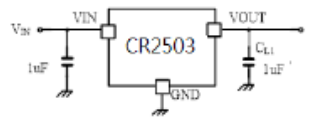


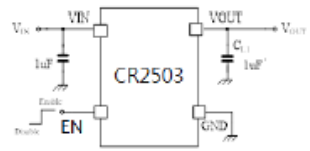
SOT23-3 SOT23-5



DFN1X1-4L DFN1.5X1.5-6L

Typical Application Circuit





Ceramic Capacitor Stable

LDO 規格書介紹

引腳定義(Pin Assignment)

詳細說明每個引腳的名稱、功能以及各封裝引腳順序

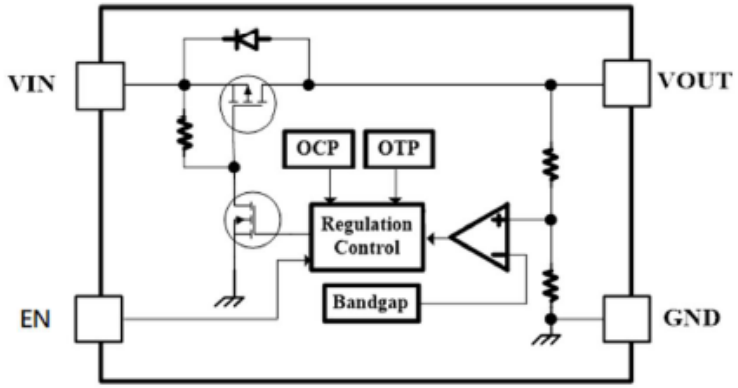
功能方塊圖(Function Block Diagram)

IC內部各功能模塊及其相互關係示意圖

Pin Assignment

Pin Name	Pin No. SOT23-3	Pin No. SOT23-5	Pin No. DFN1X1	Pin No. DFN1.5X1.5	Pin Function
VOUT	2	5	1	1	Output Voltage Pin
GND	1	2	2	3	Ground
VIN	3	1	4	6	Input Voltage pin.
EN	--	3	3	4	Enable

Function Block Diagram



LDO 規格書介紹

絕對最大額定值(Absolute Maximum Ratings)

IC在不損傷情況下所能承受的最大電壓和環境參數。

建議操作條件(Recommended Operating Conditions

IC正常操作下電壓和環境參數範圍。

電氣特性(Electrical Characteristics)

IC在建議操作條件下的各項性能參數，如電壓、電流、功耗、保護功能等。

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CR2503

Absolute Maximum Ratings (Note1)

- V_{IN} ---------- -0.3V to +6.5V
- Power Dissipation, PD@T_A=25℃, SOT23-3 ---------- 0.4W
- Thermal Resistance, θ_{JA}, SOT23-3 ---------- 250℃/W
- Power Dissipation, PD@T_A=25℃, SOT23-5 ---------- 0.45W
- Thermal Resistance, θ_{JA}, SOT23-5 ---------- 218.1℃/W
- Power Dissipation, PD@T_A=25℃, DFN1X1 ---------- 0.44W
- Thermal Resistance, θ_{JA}, DFN1X1 ---------- 226℃/W
- Power Dissipation, PD@T_A=25℃, DFN1.5X1.5 ---------- 0.67W
- Thermal Resistance, θ_{JA}, DFN1.5X1.5 ---------- 149℃/W
- Junction Temperature ---------- 125°C
- Lead Temperature (Soldering, 10 sec.) ---------- 300°C
- Storage Temperature ---------- –65°C to 150°C

Recommended Operating Conditions

- Input Voltage, V_{IN} ---------- +2.5V to +6V
- Junction Temperature ---------- -40°C to 125°C
- Ambient Temperature ---------- -40°C to 85°C

Electrical Characteristics

V_{IN} = V_{OUT} + 1V, I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1uF, T_J = 25℃, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Voltage Accuracy	ΔV_{OUT}		-2%		2%	V
Line Regulation	ΔV_{LINE}	V_{IN} = V_{OUT} + 1V to 5.5V		0.6	1.5	%
Load Regulation	ΔV_{LOAD}	I_{OUT} = 1mA to 150mA			1	%
		I_{OUT} = 1mA to 300mA			3	
Dropout Voltage	V_{DROP}	I_{OUT} = 100mA, V_{OUT} = 3.3V		130		mV
		I_{OUT} = 300mA, V_{OUT} = 3.3V		500		mV
Quiescent Current	I_Q	T_J= 25°C		0.5	1	uA
Current Limit	I_{CL}		360	560		mA
Enable high level	V_{ENHI}		0.6			V
Enable low level	V_{ENLO}				0.2	V
Power-supply rejection ratio	PSRR	f = 1kHz		60		dB
Thermal Shutdown	T_{SD}			150		°C
Thermal Shutdown Hy	T_{SDHY}			20		°C

LDO 規格書介紹

典型特性(Typical Characteristics)

IC在不同工作條件下的性能曲線圖，如輸入電壓對輸出電壓、電源抑制比（PSRR）曲線、熱特性。

Typical Characteristics

V_{IN} = V_{OUT} + 1V, I_{OUT} = 1mA, V_{OUT} = 3.3V, C_{IN} = C_{OUT} = 1uF, T_J = 25℃, unless otherwise specified

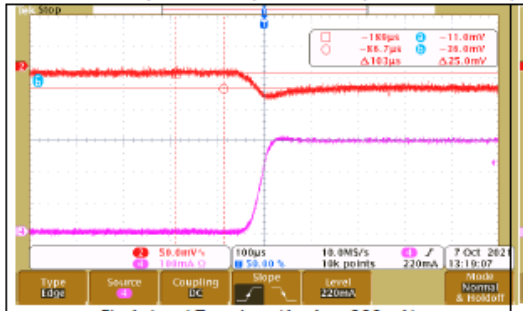


Fig 1. Load Transient (1mA to 300mA)

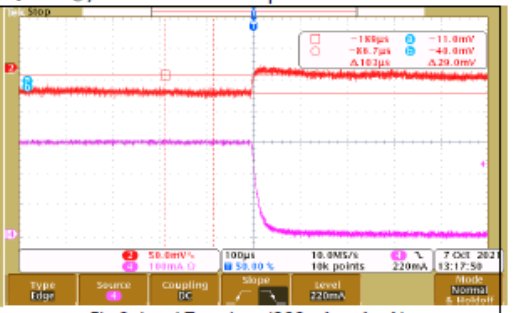


Fig 2. Load Transient (300mA to 1mA)

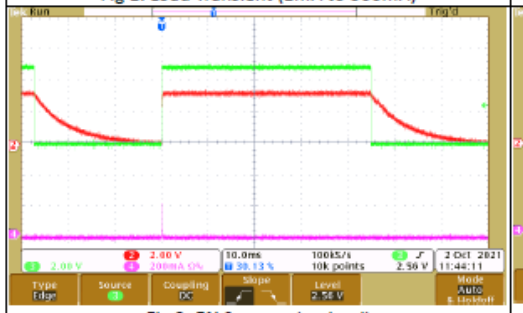


Fig 3. EN Start up (no load)

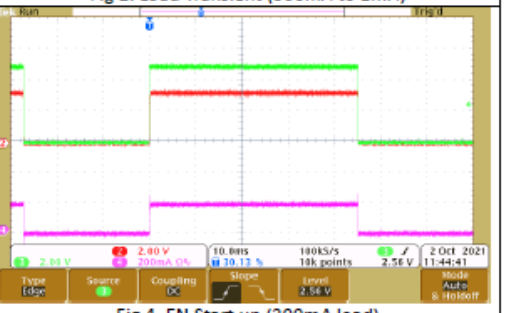


Fig 4. EN Start up (200mA load)

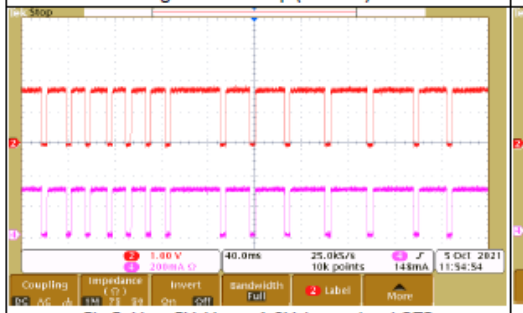


Fig 5. V_{IN} = 5V, V_{OUT} = 1.8V, heavy load OTP

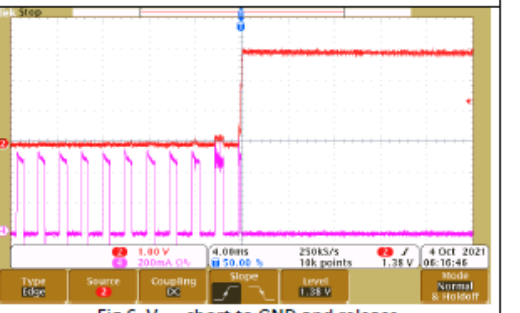


Fig 6. V_{OUT} short to GND and release

LDO 規格書介紹

IC操作資訊(IC Operation Information)

解說IC的工作原理、模式和操作注意事項。

IC應用資訊(IC Application Information)

應用端使用的建議配置以及規範事項。

IC Operation Information

Basic Operation

The CR2503 is a high performance positive low dropout (LDO) regulator designed for applications requiring very low dropout voltage, ultra-high Power Supply Ripple Rejection (PSRR), low noise and low quiescent current that can supply up to 300mA output current. The input voltage range is from 2.5V to 6V. The CR2503 features a precise 2% output regulation. The output voltage is available from 1.2V to 5.0V in 100mV steps.

The minimum required output capacitance for stable operation is 1uF (X5R or X7R) effective capacitance after consideration of the temperature and voltage coefficient of the capacitor.

Enable and Shutdown Operation

The CR2503 goes into shutdown mode when the EN pin is in a logic low condition. In this condition, the pass transistor, error amplifier, and bandgap are all turned off, reducing the supply current to only 0.1uA (max.). If the shutdown mode is not required, the EN pin can be directly tied to VIN pin to keep the LDO on.

Over-Temperature Protection (OTP)

The over-temperature protection function will turn off the P-MOSFET when the junction temperature exceeds 150℃ (typ.). Once the junction temperature cools down by approximately 20℃ (typ.), the regulator will automatically resume operation.

Current-limit Protection

The CR2503 provides current limit function to prevent the device from damages during overload or shorted-circuit condition. This current is detected by an internal sensing transistor.

Error Amplifier

The Error Amplifier compares the internal reference voltage with the output feedback voltage from the internal divider, and controls the Gate voltage of P-MOSFET to support good line regulation and load regulation at output voltage.

Output Automatic Discharge

The CR2503 output employs an internal 2KΩ (typ.) pulldown resistance to discharge the output when the EN pin is low, and the device is disabled.

IC Application Information

Like any low dropout linear regulator, the CR2503s external input and output capacitors must be properly selected for stability and performance. Use a 1μF (X5R or X7R) or larger input capacitor and place it close to the IC's VIN and GND pins. Any output capacitor meeting the minimum 1mΩ ESR (Equivalent Series Resistance) and effective capacitance larger than 1μF (X5R or X7R) requirement may be used. Place the output capacitor close to the IC's VOUT and GND pins. Increasing capacitance and decreasing ESR can improve the circuit's PSRR and line transient response.

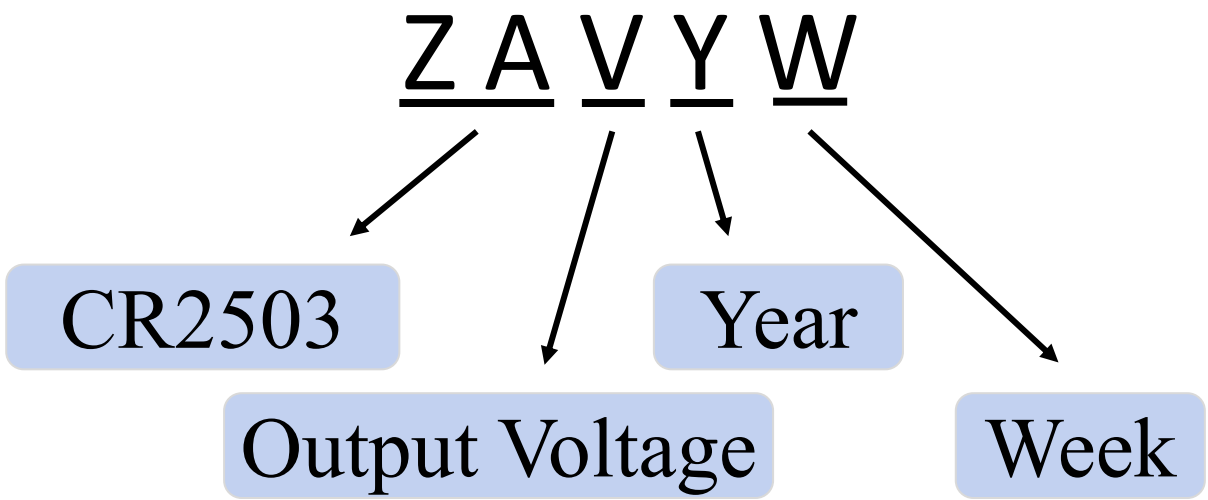
Enable Operation

The CR2503 has an EN pin to turn on or turn off the regulator, When the EN pin is in logic high, the regulator will be turned on. The shutdown current is almost 0μA typical. The EN pin may be directly tied to VIN to keep the part on. The Enable input is CMOS logic and cannot be left floating.

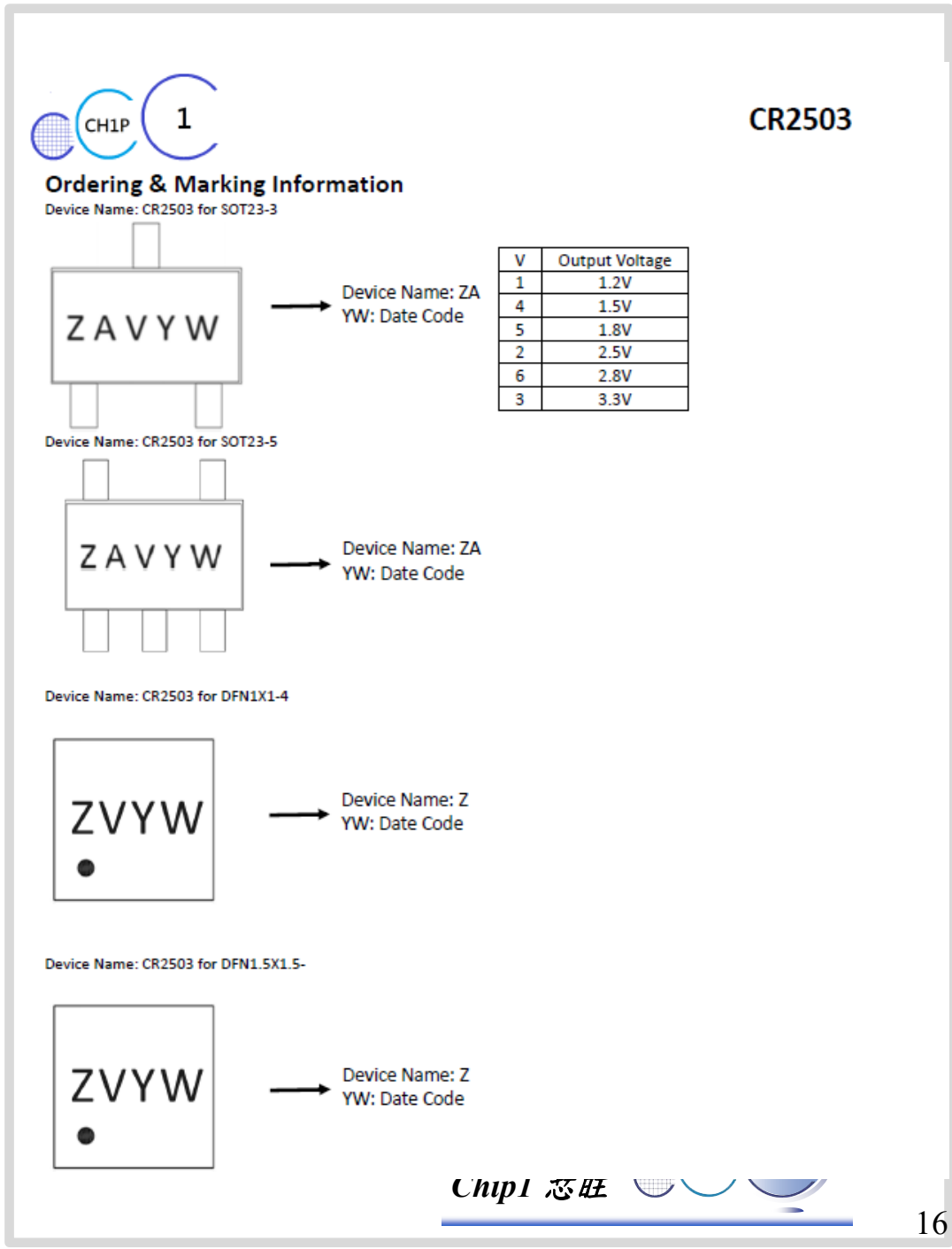
LDO 規格書介紹

訂購與標記資訊(Ordering & Marking Information)

各封裝Marking標示方式。



Note:以實際規格書命名規格為準



LDO 規格書介紹

封裝資訊(Package Information)

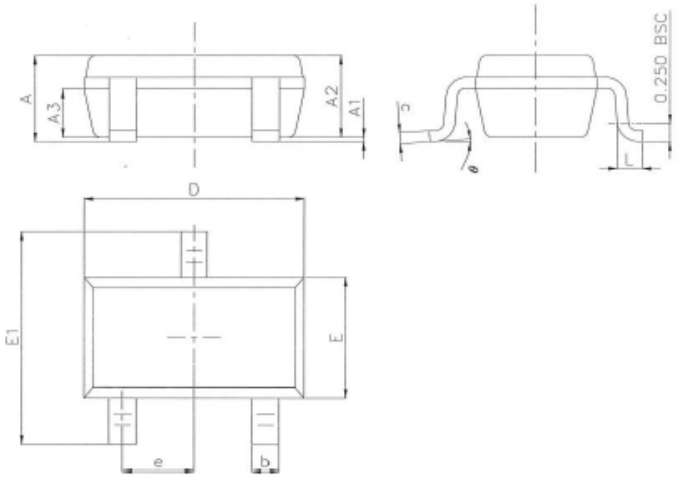
詳細描述IC物理封裝尺寸、形狀和引腳排列。

CH1P 1

CR2503

Package Information

SOT23-3



Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	1.050	1.150	1.250
A1	0.000	0.060	0.100
A2	1.000	1.100	1.200
A3	0.550	0.650	0.750
D	2.820	2.920	3.020
E1	1.510	1.610	1.700
E	2.650	2.800	2.950
b	0.300	0.400	0.500
e	0.950BSC		
θ	0°	4°	8°
L	0.300	0.420	0.570
c	0.100	0.152	0.200

Outline

- IC 基礎概論
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- LDO 規格書介紹
- **LDO 選擇原則**

LDO 選擇原則

九項重點

項目	選擇重點	目的
1	最大輸入電壓 (Maximum Input Voltage)	元件可承受系統中的最高輸入電壓，避免過壓損壞。
2	最大輸出電流 (Maximum Output Current)	可提供負載所需的最大工作電流。
3	輸出電壓精度 (Output Voltage Accuracy)	輸出電壓維持在規格範圍內，滿足系統精度需求。
4	壓差電壓 (Dropout Voltage)	在低輸入與輸出壓差下仍能維持穩定輸出，有助於提升電源效率。
5	線性調節 (Line Regulation)	輸入電壓變化時，仍能維持穩定的輸出電壓。
6	負載調節 (Load Regulation)	負載電流變化時，仍能維持穩定的輸出電壓。
7	靜態電流 (Quiescent Current)	降低元件本身的待機功耗，提升整體系統電源效率。
8	輸出雜訊 & 電源抑制比 (Output Noise & PSRR)	降低輸出雜訊並抑制輸入電源干擾，提升系統穩定性與訊號品質。
9	封裝 (Package)	根據散熱能力、PCB 空間與應用環境選擇合適封裝。

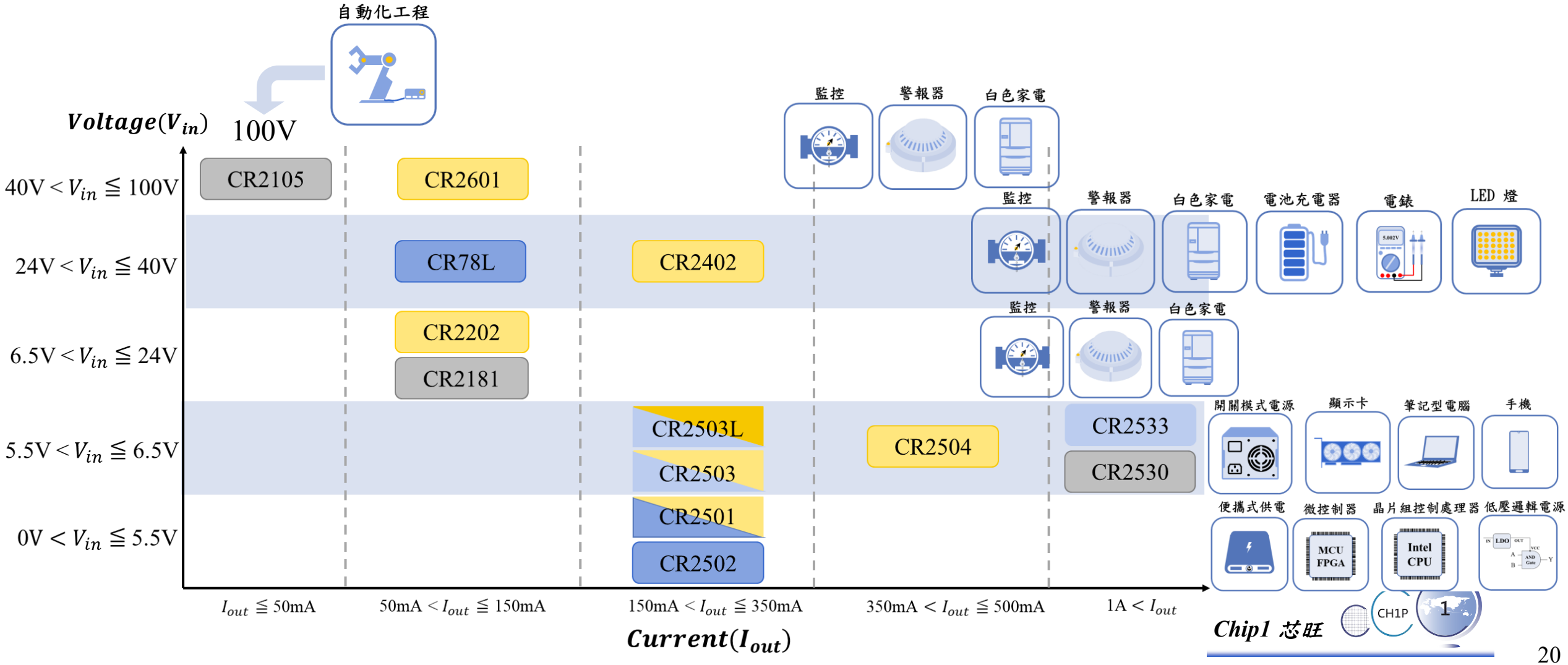
LDO 選擇原則

I_Q ≦ 0.5uA　PSRR (1kHz)≧75dB

1uA≦ I_Q ≦ 5uA　PSRR (1kHz)≧60dB

通用型

應用場景與選擇



Chip1 芯旺

LDO 選擇原則

封裝散熱	接面溫度 T_C	環境溫度 T_A
芯片溫度 T_J	熱阻θ	PCB 佈局

Package 封裝

SOT23-3 SOT23-5	DFN1X1	SOT89-3 SOT89-5	DFN3X3	QFN3.5X3.5	SOP8-EP	QFN5X5
PD≒0.4W~0.5W	PD≒0.4W~0.5W	PD≒1.0W~2.0W	PD≒1.0W~2.0W	PD≒1.0W~2.0W	PD≒1.8W~3.0W	PD≒2.0W~3.0W
CR78L	CR78L	CR78L	CR78L	CR78L	CR78L	CR78L
CR2105	CR2105	CR2105	CR2105	CR2105	CR2105	CR2105
CR2181	CR2181	CR2181	CR2181	CR2181	CR2181	CR2181
CR2202	CR2202	CR2202	CR2202	CR2202	CR2202	CR2202
CR2402	CR2402	CR2402	CR2402	CR2402	CR2402	CR2402
CR2501	CR2501	CR2501	CR2501	CR2501	CR2501	CR2501
CR2502	CR2502	CR2502	CR2502	CR2502	CR2502	CR2502
CR2503	CR2503	CR2503	CR2503	CR2503	CR2503	CR2503
CR2503L	CR2503L	CR2503L	CR2503L	CR2503L	CR2503L	CR2503L
CR2504	CR2504	CR2504	CR2504	CR2504	CR2504	CR2504
CR2530	CR2530	CR2530	CR2530	CR2530	CR2530	CR2530
CR2533	CR2533	CR2533	CR2533	CR2533	CR2533	CR2533
CR2601	CR2601	CR2601	CR2601	CR2601	CR2601	CR2601

LDO 選擇原則

封裝散熱	接面溫度 T_C	環境溫度 T_A
芯片溫度 T_J	熱阻θ	PCB 佈局

Package 封裝

SOT23-3 SOT23-5	DFN1X1	SOT89-3 SOT89-5
PD≒0.4W~0.5W	PD≒0.4W~0.5W	PD≒1.0W~2.0W
CR78L	CR78L	CR78L
CR2105	CR2105	CR2105
CR2181	CR2181	CR2181
CR2202	CR2202	CR2202
CR2402	CR2402	CR2402
CR2501	CR2501	CR2501
CR2502	CR2502	CR2502
CR2503	CR2503	CR2503
CR2503L	CR2503L	CR2503L
CR2504	CR2504	CR2504
CR2530	CR2530	CR2530
CR2533	CR2533	CR2533
CR2601	CR2601	CR2601

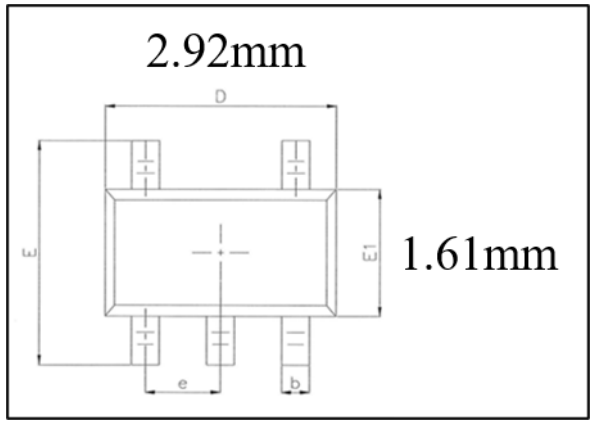
- Power Dissipation, PD@T_A=25℃, SOT23-5----------0.45W
- Thermal Resistance, θ_{JA}, SOT23-5----------218.1℃/W

θJA=218.1°C/W

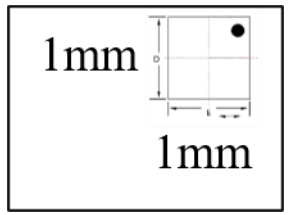
TJ=-40°C~125°C

PD=(125°C-25°C)/218.1°C=0.45W

PD=(6V-2.8V)*0.3A=0.96W,　PD=(3.8V-2.8V)*0.3A=0.3W



SOT23-5



DFN1X1-4L

Thanks for Watching