120V 50mA Ultralow-Quiescent-Current LDO

General Description

The CR2125 ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. With less than 2.4μA quiescent current at no load, the CR2125 is ideally suited for standby micro-control-unit systems, especially for always-on applications like E-meters, fire alarms, smoke detectors and other battery operated systems. The CR2125 retains all of the features that are common to low dropout regulators including a low dropout PMOS pass device, short circuit protection, and thermal shutdown.

The CR2125 has a 130-V maximum operating voltage limit, a -40°C to 125°C operating temperature range, and ±2% output voltage tolerance over the entire output current, input voltage range. The CR2125 is available in a SOT893, PSOP8 surface mount packages.

Ordering Information

Part Number	Package	XX: Output Voltage
CR2125_XX_ES8	PSOP8	25: 2.5V 33: 3.3V 50: 5.0 90: 9.0V A2: 12V
CR2125_XX_893A	SOT89-3	
CR2125_XX_893B	SOT89-3	
CR2125_XX_893C	SOT89-3	
CR2125_XX_893D	SOT89-3	

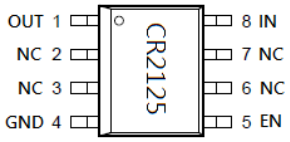
Features

- VIN Range 4.2V to 120V
- Output Voltage Tolerances of ±2%e
- Output Current of 50 mA
- Ultra Low Quiescent Current (IQ = 2.4 μA)
- Dropout Voltage Typically 4V at IOUT = 50 mA
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limit
- Ceramic Capacitor Stable

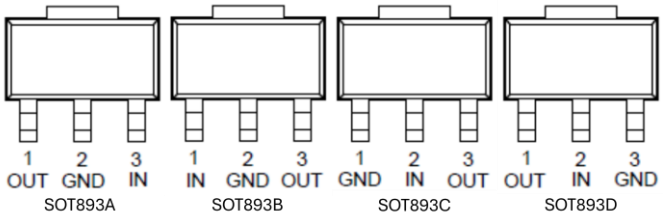
Applications

- E-meters, Water Meters and Gas Meters
- Fire Alarm, Smoke Detector
- Appliances and White Goods

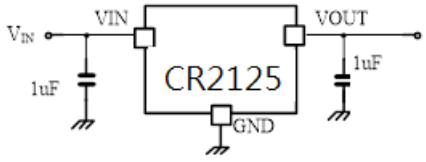
Pin Configuration

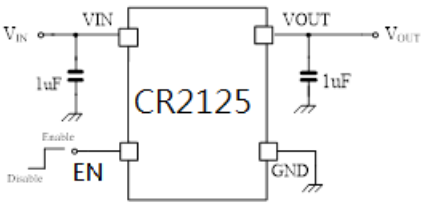


PSOP8



Typical Application Circuit



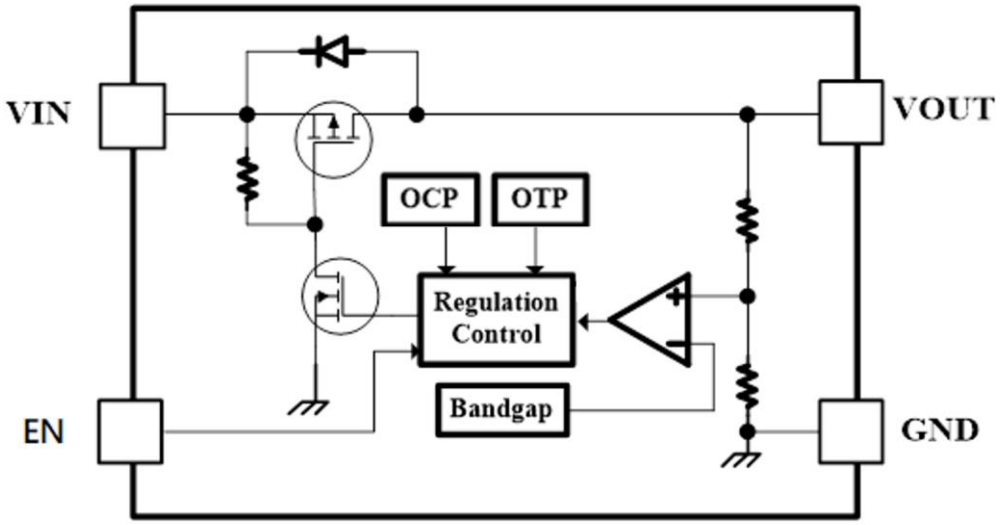


Ceramic Capacitor Stable

Pin Assignment

Pin Name	Pin No. PSOP8	Pin No. SOT893A	Pin No. SOT893B	Pin No. SOT893C	Pin No. SOT893D	Pin Function
VOUT	1	1	3	3	1	Output Voltage Pin
GND	4	2, 4	2, 4	1	3	Ground
VIN	8	3	1	2, 4	2, 4	Input Voltage pin.
EN	5	--	--	--	--	Enable

Function Block Diagram



Absolute Maximum Ratings (Note1)

- V_{IN} ---------- -0.3V to +130V
- V_{OUT} ---------- -0.3V to +26V
- EN ---------- -0.3V to +130V
- Power Dissipation, PD@T_A=25℃, PSOP-8---------- 1.8W
- Thermal Resistance, θ_{JA}, PSOP-8---------- 55℃/W
- Power Dissipation, PD@T_A=25℃, SOT89-3----------1.8W
- Thermal Resistance, θ_{JA}, SOT89-3----------55℃/W
- Junction Temperature---------- 150°C
- Lead Temperature (Soldering, 10 sec.)---------- 300°C
- Storage Temperature ---------- –65°C to 150°C

ESD Rating

- HBM(per ANSI/ESDA/JEDEC JS-001) ---------- 2KV

Recommended Operating Conditions

- Input Voltage, V_{IN} ---------- +3.3V to +120V
- Enable Voltage, V_{EN} ---------- 0V to 120V
- Junction Temperature ---------- -40°C to 125°C
- Ambient Temperature ---------- -40°C to 85°C

Electrical Characteristics

V_{IN}=V_{OUT} + 4.5V, or V_{IN}=5V(whichever is greater), I_{OUT}=100uA, C_{IN}=C_{OUT}=1.0uF, T_J=25℃, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage	V_{IN}		3.3		120	V
Output Voltage	V_{OUT}		-2%		2%	V
Line Regulation	$\triangle V_{LINE}$	V_{IN}=V_{OUT} + 1V to 120V		5	20	mV
Load Regulation	$\triangle V_{LOAD}$	I_{OUT}= 1mA to 20mA		10	25	mV
		I_{OUT}= 1mA to 50mA		20	50	
Dropout Voltage	V_{DROP}	I_{OUT}=50mA		4		V
Quiescent Current	I_Q	T_J= 25℃		2.4	4.0	uA
Shutdown Current	I_{SD}	V_{EN} =0V			0.1	uA
Current Limit	I_{CL}		55	120		mA
Enable high level	V_{ENHI}		1.0			V
Enable low level	V_{ENLO}				0.4	V
Enable pin pull high current	I_{EN}			0.02		uA
Thermal Shutdown	T_{SD}	Shutdown, temperature rise		160		℃
		Reset, temperature fall		130		

Typical Characteristics

$V_{IN}=V_{OUT}$ + 4.5V, or V_{IN}=5V(whichever is greater), I_{OUT}=100uA V_{OUT}=3.3V, $C_{IN}=C_{OUT}$=1uF, T_J=25℃, unless otherwise specified

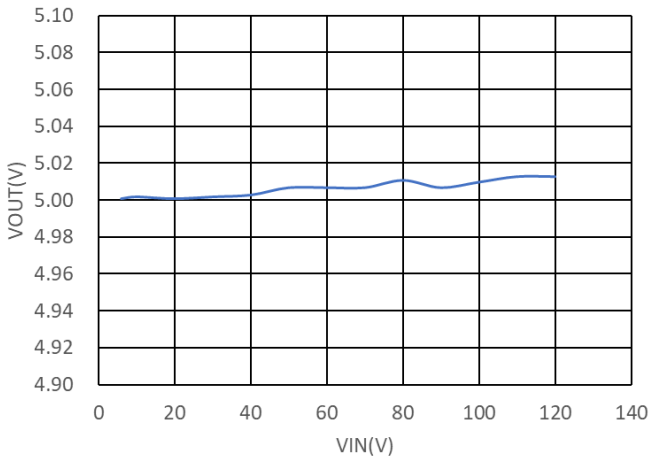


Fig 1 Vout vs Vin

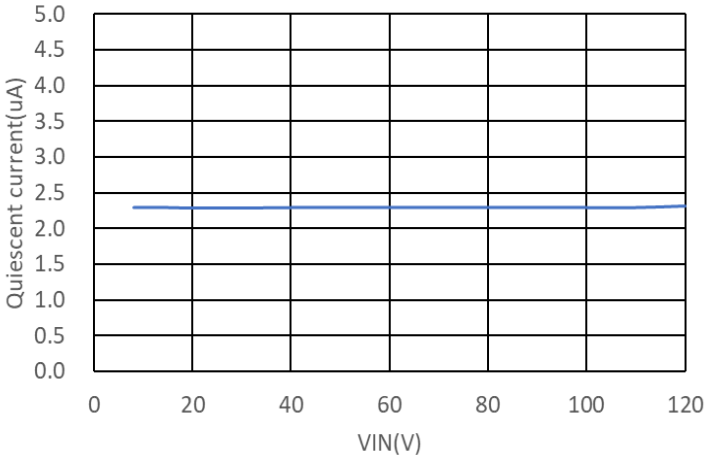


Fig 2 Iq vs Vin

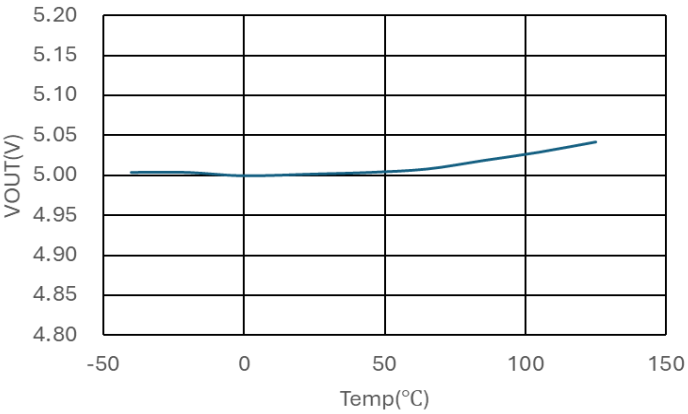


Fig 3 Vout vs Temperature

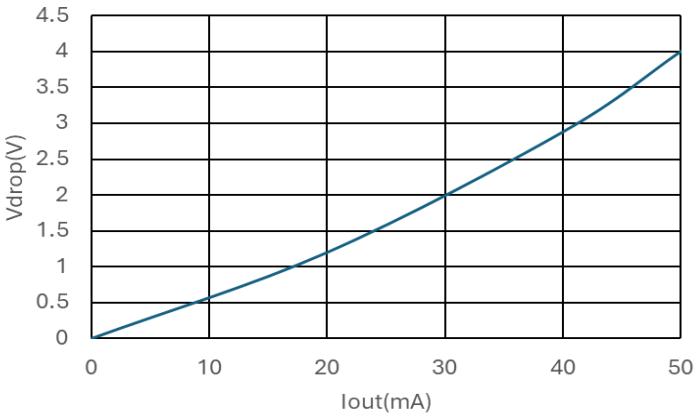


Fig 4 Dropout vs Load

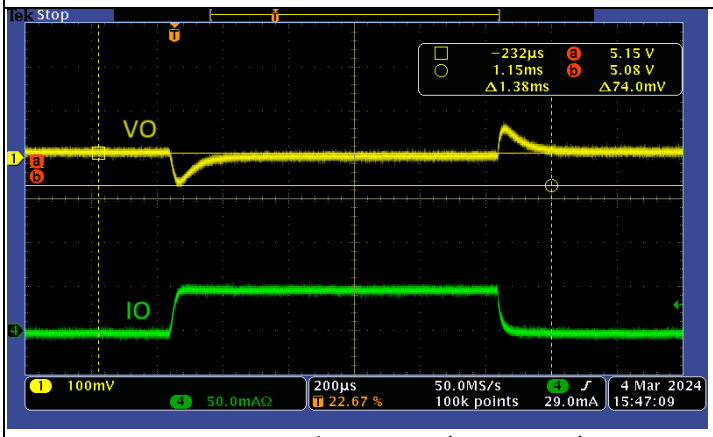


Fig 5 Vout Load Transient (1 to 50mA)

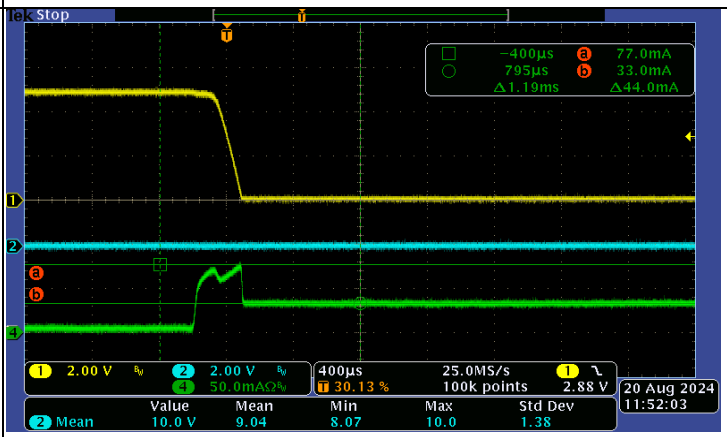


Fig 6 Vout Short to GND

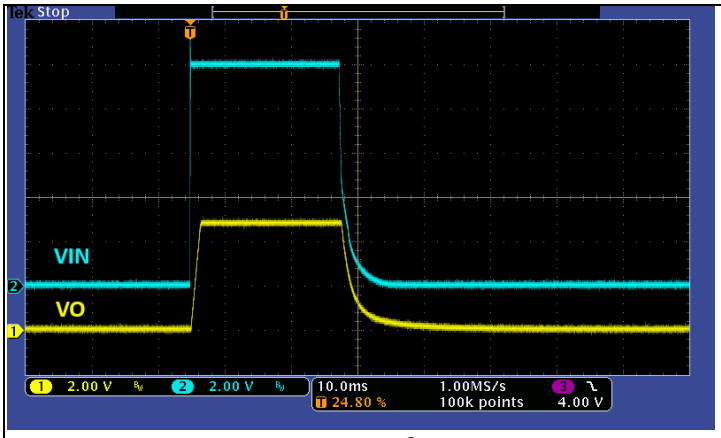


Fig 9 Vin ON & OFF

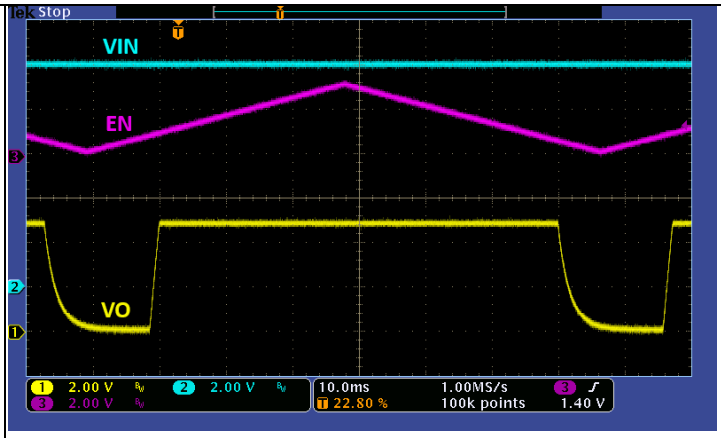


Fig 10 EN ON & OFF

IC Operation Information

Basic Operation

The CR2125 device belongs to a new generation of linear regulators that use an innovative BCD process technology to achieve very high maximum input and output voltages.

This process not only allows the CR2125 device to maintain regulation during very fast high-voltage transients up to 120 V, but it also allows the CR2125 device to regulate from a continuous high-voltage input rail. Unlike other regulators created using bipolar technology, the ground current of the CR2125 device is also constant over its output current range, resulting in increased efficiency and lower power consumption.

These features, combined with a high thermal performance SOP8EP Power PAD package, make this device ideal for industrial and telecom applications.

Over-Temperature Protection (OTP)

The over-temperature protection function will turn off the P-MOSFET when the junction temperature exceeds 160℃ (typ.). Once the junction temperature cools down by approximately 30℃(typ.), the regulator will automatically resume operation.

Current-limit Protection

The CR2125 provides current limit function to prevent the device from damages during overload or shorted-circuit condition. This current is detected by an internal sensing transistor.

Error Amplifier

The Error Amplifier compares the internal reference voltage with the output feedback voltage from the internal divider, and controls the Gate voltage of P-MOSFET to support good line regulation and load regulation at output voltage.

Enable Function

The CR2125 device provides an enable pin (EN) feature that turns on the regulator when VEN > 1.0V, and disables the regulator when VEN < 0.4V.

IC Application Information

Like any low dropout linear regulator, the CR2125's external input and output capacitors must be properly selected for stability and performance. Use a 1μF (X5R or X7R) or larger input capacitor and place it close to the IC's VIN and GND pins. Any output capacitor meeting the minimum 1mΩ ESR (Equivalent Series Resistance) and effective capacitance larger than 1μF (X5R or X7R) requirement may be used. Place the output capacitor close to the IC's VOUT and GND pins. Increasing capacitance and decreasing ESR can improve the circuit's PSRR and line transient response.

Current Limit

The CR2125 contains an independent current limiter, which monitors and controls the pass transistor's gate voltage, limiting the output current to 0.12A (typ.). The output can be shorted to ground indefinitely without damaging the part.

Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at specific output current. The dropout voltage V_{DROP} can also be expressed as the voltage drop on the pass-FET at specific output current (I_{RATED}) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized as an resistance $R_{DS(ON)}$. Thus the dropout voltage can be defined as ($V_{DROP} = V_{VIN} - V_{VOUT} = R_{DS(ON)} \times I_{RATED}$). For normal operation, the suggested LDO operating range is ($V_{VIN} > V_{VOUT} + 4.5V$) for good transient response and PSRR ability. Conversely, operating at the ohmic region will degrade these performance severely.

Minimum Operating Input Voltage (VIN)

The CR2125 lacks dedicated UVLO circuitry. The CR2125 requires a minimum input voltage of 5V. The output voltage is not regulated until VIN has reached at least the greater of 5 V or (VOUT + 4.5V).

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$ and

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance. For recommended operating condition specifications the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP8 (Exposed PAD) package, the thermal resistance, θ_{JA}, is 55°C/W on a standard JEDEC 51-7 four-layer thermal test board. For SOT893 package, the thermal resistance, θ_{JA}, is 55°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)} = (125°C - 25°C) / (55°C/W) = 1.81W$ for SOP8 (Exposed Pad) package

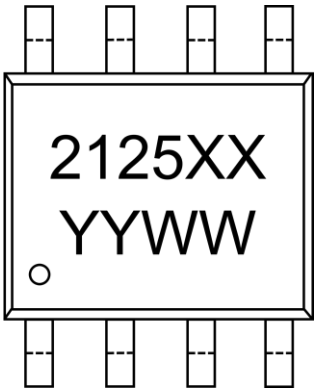
$P_{D(MAX)} = (125°C - 25°C) / (55°C/W) = 1.81W$ for SOT893 package The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure(below) allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

Layout Considerations

The dynamic performance of the CR2125 is dependent on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the CR2125. Best performance is achieved by placing CIN and COUT on the same side of the PCB as the CR2125, and as close to the package as possible is practical. The ground connections for C_{IN} and C_{OUT} must be back to the CR2125 ground pin using a copper trace as wide and short as possible. Connections using long trace lengths, narrow trace widths, and/or connections through vias must be avoided. These added parasitic inductances and resistance may result in inferior performance especially during transient conditions.

Ordering & Marking Information

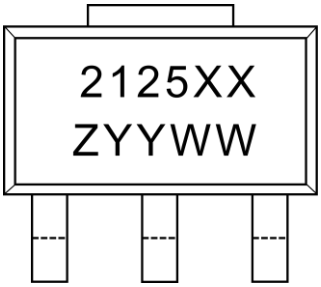
Device Name: CR2125 for PSOP8



Device Name: 2125
YYWW: Date Code

XX	Output Voltage
25	2.5V
33	3.3V
50	5.0V
90	9.0V
A2	12V

Device Name: CR2125 for SOT89-3

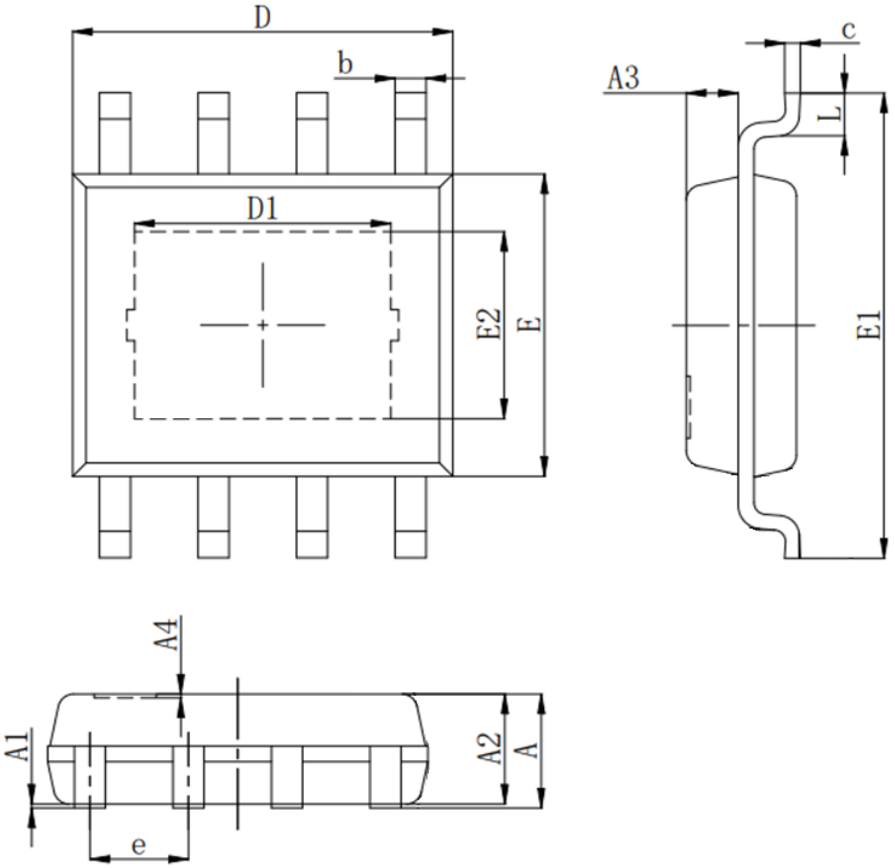


Device Name: 2125
YYWW: Date Code

Z	Package
A	SOT893A
B	SOT893B
C	SOT893C
D	SOT893D

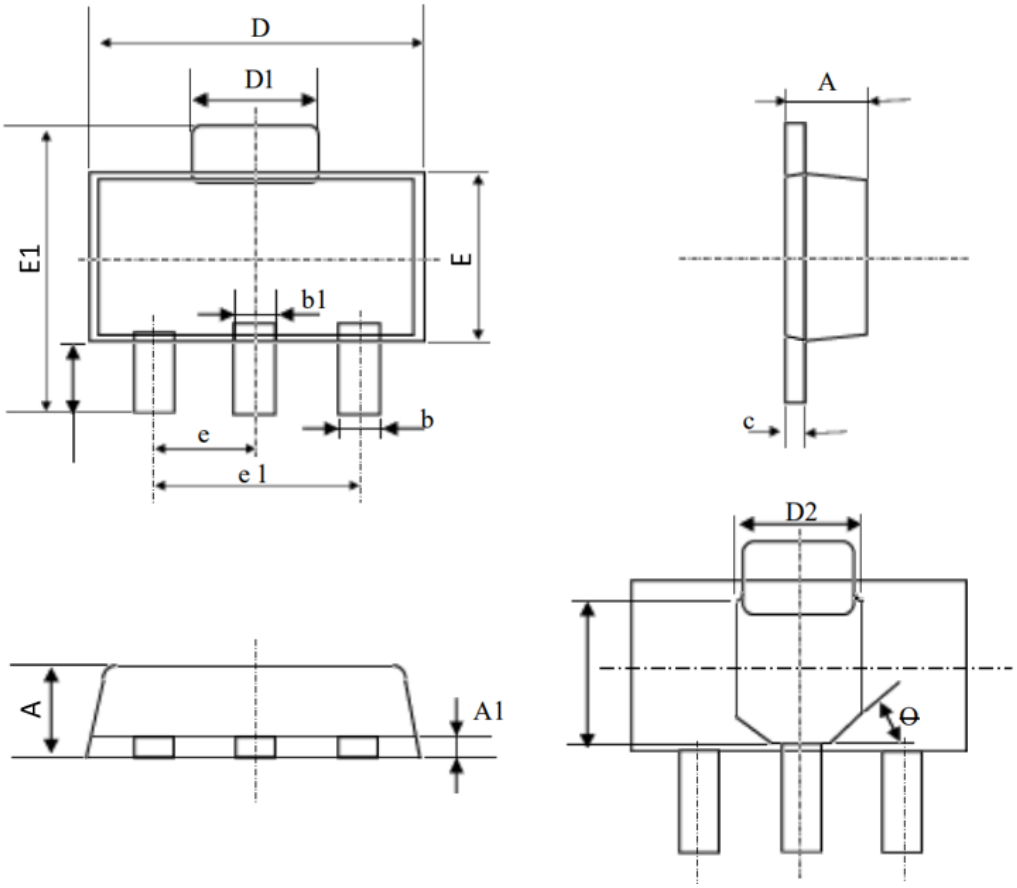
XX	Output Voltage
25	2.5V
33	3.3V
50	5.0V
90	9.0V
A2	12V

Package Information
PSOP8



Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	1.30	1.50	1.70
A1	0.00	0.10	0.15
A2	1.35	1.42	1.55
A3	0.645	0.670	0.695
A4	0.02		0.05
c	0.170	0.203	0.250
E	3.8	3.9	4.0
E1	5.80	6.00	6.20
E2	2.183	2.283	2.383
L	0.45	0.60	0.75
b	0.33	0.40	0.51
D	4.80	4.90	5.00
D1	3.272	3.372	3.472
e		1.27	

Package Information
SOT89-3



Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	1.40	1.50	1.60
A1	0.30	0.40	0.50
L	0.8	1.00	1.20
b	0.35	0.40	0.45
b1	0.40	0.48	0.55
c	0.30	0.40	0.5
D	4.40	4.50	4.6
D1	1.60	1.70	1.80
D2		1.72	
E	2.40	2.50	2.60
E1	3.94	4.10	4.25
E2 e e1 θ		1.9 1.5 3.0 45°	