

CL74AUP1G126 Single Bus Buffer Gate With 3-State Output

General Description

The single buffer is designed for 1.65-V to 5.5-V VCC operation.

The CL74AUP1G126 device is a single line driver with a 3-state output. The output is disabled when the output-enable input is low.

The CL74AUP1G126 device is available in a variety of packages, including SOT23-5, SC70.

Ordering Information

Part Number	Marking	Package
CL74AUP1G126_235	P0NXW	SOT-23-5
CL74AUP1G126_70	PNXW	SC70

Features

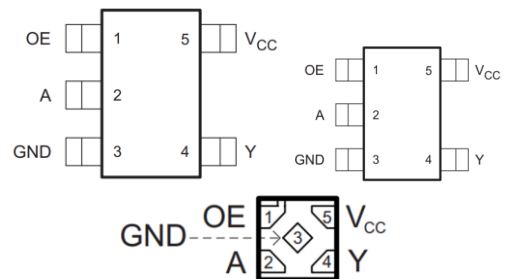
- Inputs Accept Voltages 0.8V to 3.6 V
- Max Tpd of 4.7 ns at 3.3 V
- Low Static-Consumption, 0.9- μ A Max Icc
- Low Noise Overshoot and Undershoot < 10% of Vcc
- Input-Disable Feature Allows Floating Input Conditions
- Ioff Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input ($V_{hys} = 250\text{mV}$ Typical 3.3V)
- 3.6V I/O Tolerant to Support Mixed-Mode Signal Operation
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)

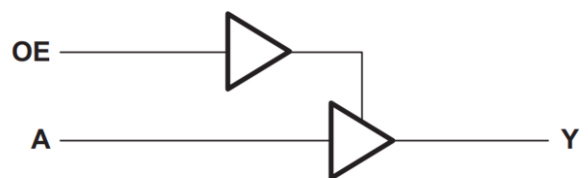
Applications

- audio Dock: Portable
- BluRay™ Players and Home Theaters
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid-State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Wireless Headsets, Keyboards and Mice

Pin Configuration



Simplified Schematic





Pin Assignment

CL74AUP1G126

Pin Name	Pin No.	Pin Function
OE	1	Input
A	2	Input
GND	3	Ground
Y	4	Output
VCC	5	Power pin

Absolute Maximum Ratings (Note1)

- V_{CC} ----- -0.5V to +4.6V
- V_I ----- -0.5V to +4.6V
- V_O (Voltage range applied to any output in the high-impedance or power-off state)----- -0.3V to +4.6V
- V_O (Voltage range applied to any output in the high or slow state)----- -0.3V to $V_{CC}+0.3V$
- Input clamp current ----- -50mA
- Output clamp current ----- -50mA
- Continuous output current ----- $\pm 20mA$
- Storage Temperature ----- $-65^{\circ}C$ to $150^{\circ}C$

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{CC}	Operating	0.8		3.6	V
Input voltage	V_I		0		3.6	V
Output voltage	V_O		0		V_{CC}	V
High- level input voltage	V_{IH}	$V_{CC} = 0.8V$	V_{CC}			V
		$V_{CC} = 1.1V$ to $1.95V$	$0.65 \times V_{CC}$			
		$V_{CC} = 2.3V$ to $2.7V$	1.6			
		$V_{CC} = 3V$ to $3.6V$	2			
Low- level input voltage	V_{IL}	$V_{CC} = 0.8V$			0	V
		$V_{CC} = 1.1V$ to $1.95V$			$0.35 \times V_{CC}$	
		$V_{CC} = 2.3V$ to $2.7V$			0.7	
		$V_{CC} = 3V$ to $3.6V$			0.9	

High- level output current	I_{OH}	$V_{CC} = 0.8V$			-20	uA
		$V_{CC} = 1.1V$			-1.1	mA
		$V_{CC} = 1.4V$			-1.7	
		$V_{CC} = 1.65V$			-1.9	
		$V_{CC} = 2.3V$			-3.1	
		$V_{CC} = 3V$			-4	
Low- level output current	I_{OL}	$V_{CC} = 0.8V$			20	uA
		$V_{CC} = 1.1V$			1.1	mA
		$V_{CC} = 1.4V$			1.7	
		$V_{CC} = 1.65V$			1.9	
		$V_{CC} = 2.3V$			3.1	
		$V_{CC} = 3V$			4	
Input transition rise or fall rate	$\Delta T/\Delta V$	$V_{CC} = 0.8V$ to $3.6V$			200	ns/V
Operating temperature	T_A		-40		85	°C

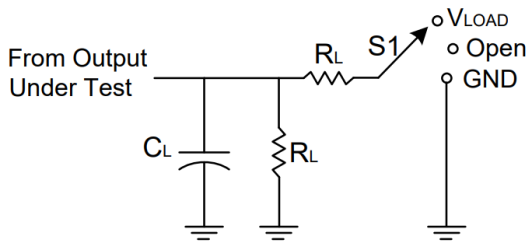
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
High- level output voltage	V_{OH}	$V_{CC} = 0.8\sim 3.6V, I_{OH} = -20\mu A$	$V_{CC}-0.1$			V
		$V_{CC} = 1.1V, I_{OH} = -1.1mA$	$0.75 \times V_{CC}$			
		$V_{CC} = 1.4V, I_{OH} = -1.7mA$	1.11			
		$V_{CC} = 1.65V, I_{OH} = -1.9mA$	1.32			
		$V_{CC} = 2.3V, I_{OH} = -2.3mA$	2.05			
		$V_{CC} = 2.3V, I_{OH} = -3.1mA$	1.9			
		$V_{CC} = 3V, I_{OH} = -2.7mA$	2.72			
		$V_{CC} = 3V, I_{OH} = -4mA$	2.6			
Low- level output voltage	V_{OL}	$V_{CC} = 0.8\sim 3.6V, I_{OL} = 20\mu A$			0.1	V
		$V_{CC} = 1.1V, I_{OL} = 1.1mA$			$0.3 \times V_{CC}$	
		$V_{CC} = 1.4V, I_{OL} = 1.7mA$			0.31	
		$V_{CC} = 1.65V, I_{OL} = 1.9mA$			0.31	
		$V_{CC} = 2.3V, I_{OL} = 2.3mA$			0.31	
		$V_{CC} = 2.3V, I_{OL} = 3.1mA$			0.44	
		$V_{CC} = 3V, I_{OL} = 2.7mA$			0.31	
		$V_{CC} = 3V, I_{OL} = 4mA$			0.44	
Input leakage current	I_I	$V_{IN} = 3.6V$ or GND, $V_{CC} = 0\sim 3.6V$			0.1	uA
Power off leakage current	I_{OFF}	V_I or $V_O = 0V$ to $3.6V, V_{CC} = 0V$			0.2	uA
Supply current	I_{CC}	$V_I = GND$ or (V_{CC} to $3.6V$), $I_{OUT} = 0$, $V_{CC} = 0.8\sim 3.6V$			0.5	uA
Additional supply current per input pin	ΔI_{CC}	$V_I = V_{CC} - 0.6V, I_{OUT} = 0$			40	uA

Switching Characteristics

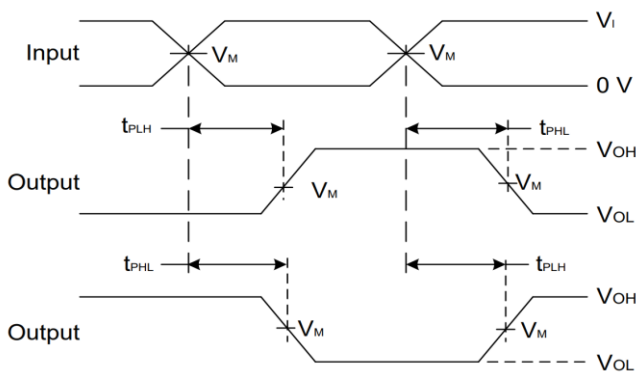
Parameter	From Input	To Output	Test Conditions	Min	Typ	Max	Units
T _{PD}	A	Y	V _{CC} = 0.8V		22.5		ns
			V _{CC} = 1.2V±0.1V,	5.8	9.3	15.1	
			V _{CC} = 1.5V±0.1V,	4.4	6.6	10.2	
			V _{CC} = 1.8V±0.15V	3.5	5.3	8.3	
			V _{CC} = 2.5V±0.2V	2.7	3.9	5.8	
			V _{CC} = 3.3V±0.3V	2.4	3.2	4.7	
T _{en}	OE	Y	V _{CC} = 0.8V		25.2		ns
			V _{CC} = 1.2V±0.1V,	7	11.3	18.1	
			V _{CC} = 1.5V±0.1V,	5.5	8.1	12.2	
			V _{CC} = 1.8V±0.15V	4.3	6.5	10.1	
			V _{CC} = 2.5V±0.2V	3.4	4.8	7.1	
			V _{CC} = 3.3V±0.3V	2.9	4.1	5.9	
T _{dis}	OE	Y	V _{CC} = 0.8V		14		ns
			V _{CC} = 1.2V±0.1V,	3.7	5.8	8.2	
			V _{CC} = 1.5V±0.1V,	5.5	3.9	5.9	
			V _{CC} = 1.8V±0.15V	3.3	4.5	6.6	
			V _{CC} = 2.5V±0.2V	2.3	3.2	4.3	
			V _{CC} = 3.3V±0.3V	2.4	4.8	6.2	

Parameter Measurement Information

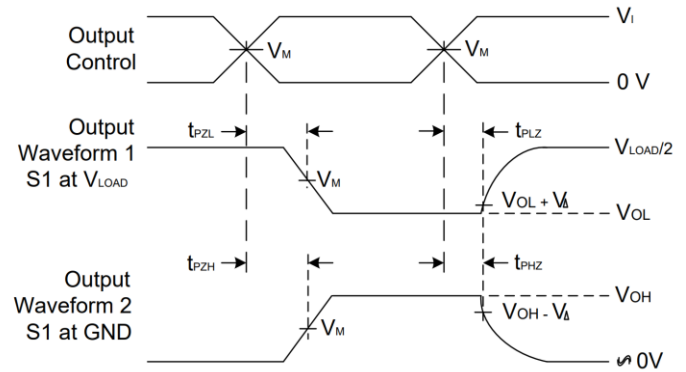


TEST	S1	RL
t_{PLH}/t_{PHL}	Open	1M Ω
t_{PLZ}/t_{PZL}	V _{LOAD}	5K Ω
t_{PHZ}/t_{PZH}	GND	5K Ω

VCC	INPUTS		V _M	V _{LOAD}	C _L	V Δ
	V _I	t _r /t _f				
0.8V	V _{CC}	$\leq 3\text{ns}$	V _{CC} /2	2 X V _{CC}	15pF	0.1V
1.2V \pm 0.1V,	V _{CC}	$\leq 3\text{ns}$	V _{CC} /2	2 X V _{CC}	15pF	0.1V
1.5V \pm 0.1V,	V _{CC}	$\leq 3\text{ns}$	V _{CC} /2	2 X V _{CC}	15pF	0.1V
1.8V \pm 0.15V	V _{CC}	$\leq 3\text{ns}$	V _{CC} /2	2 X V _{CC}	15pF	0.15V
2.5V \pm 0.2V	V _{CC}	$\leq 3\text{ns}$	V _{CC} /2	2 X V _{CC}	15pF	0.15V
3.3V \pm 0.3V	V _{CC}	$\leq 3\text{ns}$	V _{CC} /2	2 X V _{CC}	15pF	0.3V



**Voltage Waveform Propagation Delay Times
Inverting and Non Inverting Outputs**



**Voltage Waveform Enable and Disable Times
Low- and High-Level Enabling**

- Notes:
- A. C_L includes probe and jig capacitance
 - B. All pulses and supplied at pulse repetition rate $\leq 10\text{MHz}$
 - C. The Inputs are measured separately one transition per measurement
 - D. t_{PZL} and t_{PHZ} are the same as t_{dis}
 - E. t_{PZL} and t_{PZH} are the same as t_{en}
 - F. t_{PLH} and t_{PHL} are the same as t_{pD}

IC Operation Information

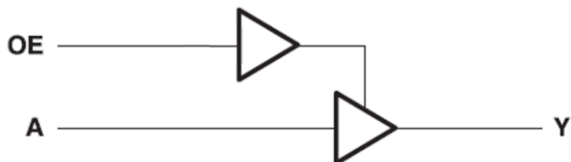
Basic Operation

The AUP family is the solution to the industry's low-power needs in battery-powered portable applications. This family of devices is specified for low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity.

This device contains one buffer gate device with output enable control and performs the Boolean function $Y = A$. This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device, which prevents damage to the device.

To assure the high-impedance state during power up or power down, OE must be tied to GND through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Function Block Diagram



Feature Description

- Wide operating voltage range.
 - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- Ioff feature allows voltages on the inputs and outputs when V_{CC} is 0 V..

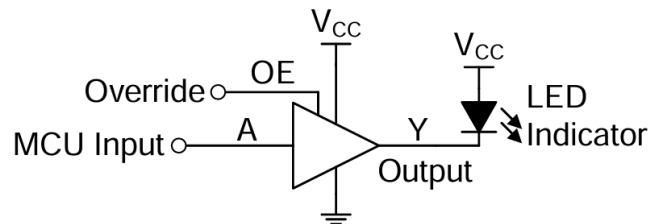
Device Functional Table

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

IC Application Information

The CL74AUP1G126 device is an output enabled CMOS buffer that can be used in LED indicator applications that require less than 4 mA. The device can produce up to 4 mA of drive current at 3.3 V. The inputs to the device are also overvoltage tolerant up to 3.6 V, allowing it to translate down to any valid V_{CC} .

Typical Application

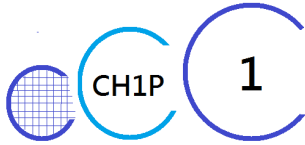


Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

Detailed Design Procedure

1. Recommended Input Conditions
 - Rise time and fall time specs. See $(\Delta t/\Delta V)$ in the Recommended Operating Conditions table.
 - Specified high and low levels. See $(V_{IH}$ and $V_{IL})$ in the Recommended Operating Conditions table.
 - Inputs are overvoltage tolerant allowing them to go as high as $(V_i \text{ max})$ in the Recommended Operating Conditions table at any valid V_{CC} .
2. Recommend Output Conditions
 - Load currents should not exceed $(I_o \text{ max})$ per output and should not exceed total current (continuous current through V_{CC} or GND) for the part. These limits are located in the Absolute Maximum Ratings table.
 - Outputs should not be pulled above V_{CC} .



CL74AUP1G126

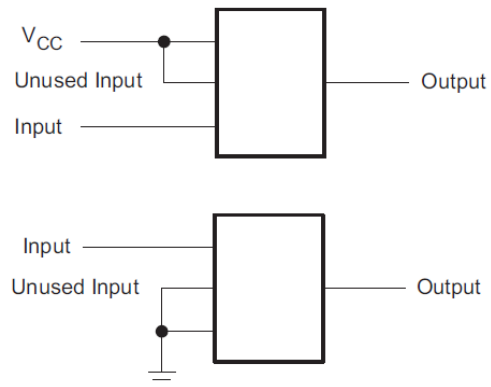
Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the Recommended Operating Conditions table.

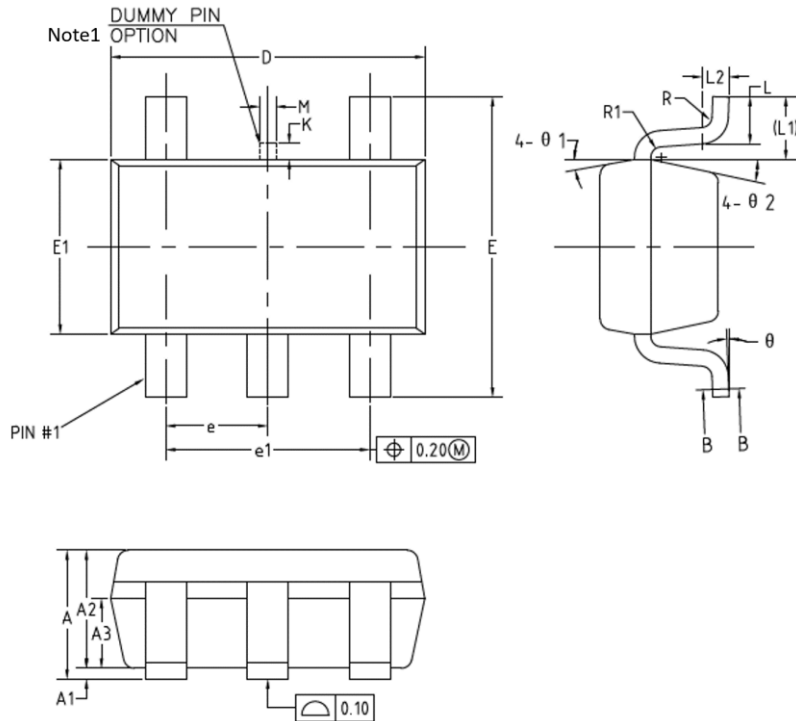
The VCC pin must have a good bypass capacitor to prevent power disturbance. TI recommends to use a 0.1- μ F capacitor for this device. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. Install the bypass capacitor as close to the power pin as possible for best results.

Layout Considerations

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient.



Package Information SOT23-5

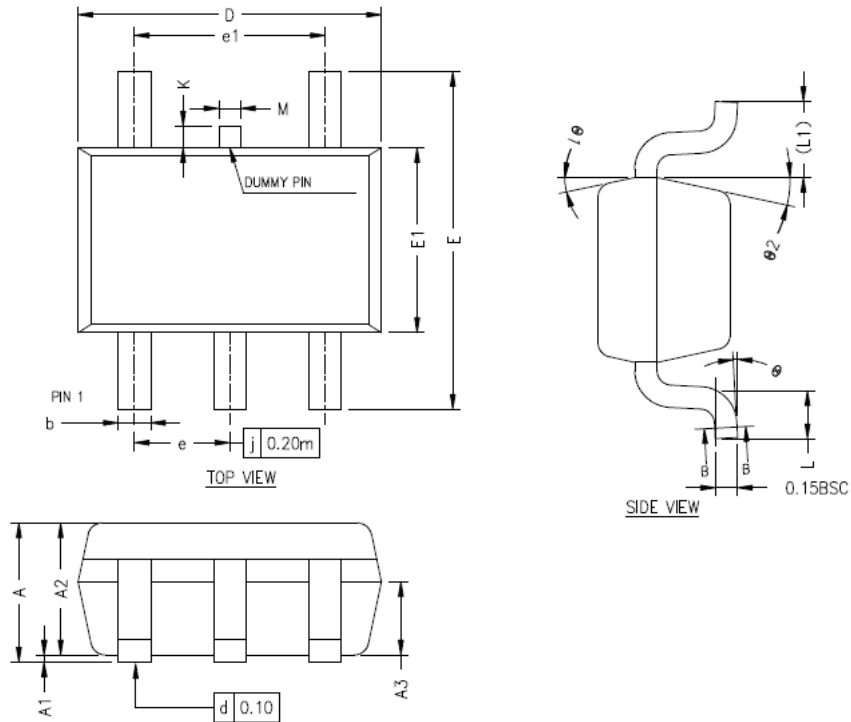


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.25
A1	0	—	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
△ b	0.34	—	0.45
△ b1	0.34	0.38	0.41
△ c	0.12	—	0.20
△ c1	0.12	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
△ E1	1.526	1.626	1.700
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
△ K	0	—	0.20
L	0.30	0.40	0.60
L1	0.59REF		
L2	0.25BSC		
△ M	0.10	0.15	0.20
R	0.05	—	0.20
R1	0.05	—	0.20
θ	0°	—	8°
θ 1	8°	10°	12°
θ 2	10°	12°	14°

Notes: 1. Dummy pin may differ or may not be present.

Package Information SC70



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	—	1.10
A1	0	—	0.10
A2	0.80	0.90	1.00
A3	0.40	0.50	0.60
b	0.17	—	0.30
b1	0.17	0.22	0.25
\triangle c	0.12	—	0.20
\triangle c1	0.12	0.15	0.16
D	2.02	2.07	2.12
E	2.20	2.30	2.40
E1	1.21	1.26	1.31
e	0.60	0.65	0.70
e1	1.20	1.30	1.40
L	0.26	0.33	0.46
L1	0.52REF		
\triangle M	0.10	0.15	0.20
\triangle K	0	—	0.20
θ	0°	—	8°
θ_1	10°	12°	14°
θ_2	10°	12°	14°