

CL74AUP1G06 Low Power Single Inverter With Open-Drain Outputs

General Description

This single inverter buffer and driver is designed for 0.8-V to 3.6-V V_{CC} operation.

The output of the CL74AUP1G06 device is open-drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

This device is fully specified for partial-power-down applications using I_{OFF} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

Ordering Information

Part Number	Marking	Package
CL74AUP1G06-235	P06XW	SOT-23-5
CL74AUP1G06-70	PDXW	SC70

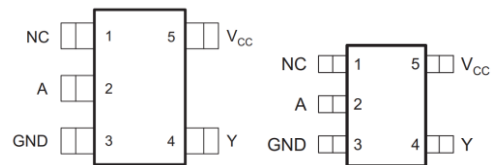
Features

- Inputs Accept Voltages 0.8V to 3.6 V
- Max Tpd of 6 ns at 3.3 V
- Low Static-Consumption, 0.9- μ A Max I_{CC}
- Low Noise Overshoot and Undershoot < 10% of V_{CC}
- I_{OFF} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input ($V_{hys} = 250\text{mV}$ Typical 3.3V)
- 3.6V I/O Tolerant to Support Mixed-Mode Signal Operation
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

Applications

- AV Receivers
- Smartphone
- Blu-ray Player and Home Theater
- Desktop or Notebook PCs
- Embedded PC
- GPS: Personal Navigation Devices
- Mobile Internet Devices
- Network Projector Front-Ends
- Portable Media Players
- Smoke Detectors
- Solid State Drive (SSD): Enterprise
- High-Definition (HDTV)
- Tablet: Enterprise
- Audio Dock: Portable

Pin Configuration



Simplified Schematic





Pin Assignment

CL74AUP1G06

Pin Name	Pin No.	Pin Function
NC	1	No connect
A	2	Input
GND	3	Ground
Y	4	Output
V _{CC}	5	Power pin

Absolute Maximum Ratings (Note1)

- V_{CC} ----- -0.5V to +4.6V
- V_I----- -0.5V to +4.6V
- V_O(Voltage range applied to any output in the high-impedance or power-off state)----- -0.3V to +4.6V
- V_O(Voltage range applied to any output in the high or slow state)----- -0.3V to V_{CC}+0.3V
- Input clamp current ----- -50mA
- Output clamp current ----- -50mA
- Continuous clamp current ----- ±20mA
- Storage Temperature ----- -65°C to 150°C

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V _{CC}	Operating	0.8		3.6	V
Input voltage	V _I		0		3.6	V
Output voltage	V _O		0		3.6	V
High- level input voltage	V _{IH}	V _{CC} = 0.8V	V _{CC}			V
		V _{CC} = 1.1V to 1.95V	0.65 x V _{CC}			
		V _{CC} = 2.3V to 2.7V	1.6			
		V _{CC} = 3V to 3.6V	2			
Low- level input voltage	V _{IL}	V _{CC} = 0.8V			0	V
		V _{CC} = 1.1V to 1.95V			0.35 x V _{CC}	
		V _{CC} = 2.3V to 2.7V			0.7	
		V _{CC} = 3V to 3.6V			0.9	

Low- level output current	I_{OL}	$V_{CC} = 0.8V$			20	uA
		$V_{CC} = 1.1V$			1.1	mA
		$V_{CC} = 1.4V$			1.7	
		$V_{CC} = 1.65V$			1.9	
		$V_{CC} = 2.3V$			3.1	
		$V_{CC} = 3V$			4	
Input transition rise or fall rate	$\Delta T/\Delta V$	$V_{CC} = 0.8V$ to $3.6V$			200	ns/V
Operating temperature	T_A		-40		85	°C

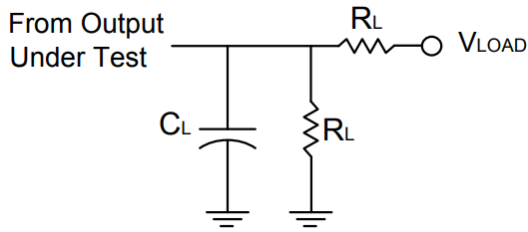
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Low- level output voltage	V_{OL}	$V_{CC} = 0.8\sim 3.6V, I_{OL} = 20\mu A$			0.1	V
		$V_{CC} = 1.1V, I_{OL} = 1.1mA$			$0.3 \times V_{CC}$	
		$V_{CC} = 1.4V, I_{OL} = 1.7mA$			0.31	
		$V_{CC} = 1.65V, I_{OL} = 1.9mA$			0.31	
		$V_{CC} = 2.3V, I_{OL} = 2.3mA$			0.31	
		$V_{CC} = 2.3V, I_{OL} = 3.1mA$			0.44	
		$V_{CC} = 3V, I_{OL} = 2.7mA$			0.31	
		$V_{CC} = 3V, I_{OL} = 4mA$			0.44	
Input leakage current	I_I	$V_{IN} = 3.6V$ or GND, $V_{CC} = 0\sim 3.6V$			0.1	uA
Power off leakage current	I_{OFF}	V_I or $V_O = 0V$ to $3.6V, V_{CC} = 0V$			0.2	uA
Supply current	I_{CC}	$V_I = GND$ or (V_{CC} to $3.6V$), $I_{OUT} = 0$, $V_{CC} = 0.8\sim 3.6V$			0.5	uA
Additional supply current per input pin	ΔI_{CC}	$V_I = V_{CC} - 0.6V, I_{OUT} = 0$			40	uA

Switching Characteristics

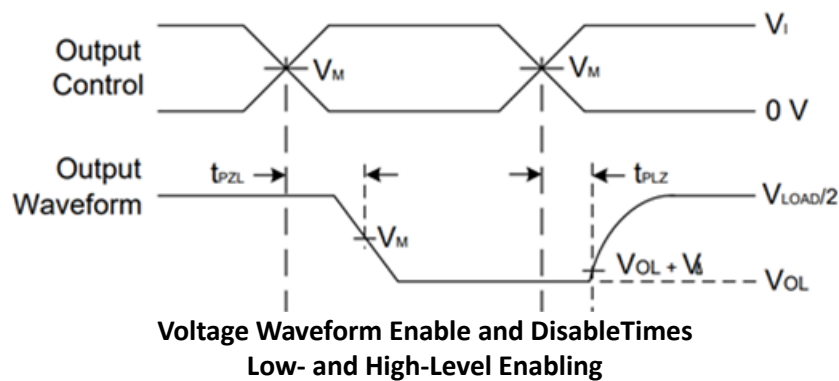
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	
Propagation delay from input(A or B) to output(Y)	T_{PD}	$V_{CC} = 0.8V$		17.4		ns	
		$V_{CC} = 1.2V \pm 0.1V,$	$C_L = 15pF$	4.9	12		12.2
		$V_{CC} = 1.5V \pm 0.1V,$		3.5	5		7.7
		$V_{CC} = 1.8V \pm 0.15V$		3.2	4.8		6.6
		$V_{CC} = 2.5V \pm 0.2V$		2.5	3.5		4.5
		$V_{CC} = 3.3V \pm 0.3V$		2	3.8		6

Parameter Measurement Information



TEST	Condition
t_{PLZ}	V_{LOAD}
t_{PZL}	V_{LOAD}

VCC	INPUTS		V_M	C_L	R_L
	V_I	t_r/t_f			
0.8V	V_{CC}	$\leq 2\text{ns}$	$V_{CC}/2$	15pF	5K Ω
$1.2\text{V} \pm 0.1\text{V}$	V_{CC}	$\leq 2\text{ns}$	$V_{CC}/2$	15pF	5K Ω
$1.5\text{V} \pm 0.1\text{V}$	V_{CC}	$\leq 2\text{ns}$	$V_{CC}/2$	15pF	5K Ω
$1.8\text{V} \pm 0.15\text{V}$	V_{CC}	$\leq 2\text{ns}$	$V_{CC}/2$	15pF	5K Ω
$2.5\text{V} \pm 0.2\text{V}$	3V	$\leq 2.5\text{ns}$	1.5V	15pF	5K Ω
$3.3\text{V} \pm 0.3\text{V}$	V_{CC}	$\leq 2.5\text{ns}$	$V_{CC}/2$	15pF	5K Ω



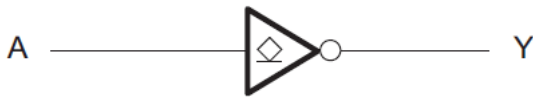
- Notes:
- A. C_L includes probe and jig capacitance
 - B. All pulses and supplied at pulse repetition rate $\leq 10\text{MHz}$
 - C. The Inputs are measured one at a time with one transition per measurement
 - D. For the open drain device t_{PLZ} and t_{PZL} are the same as t_{PD}
 - E. t_{PZL} is measured at V_M
 - F. t_{PLZ} is measured at $V_{OL} + V_{\Delta}$

IC Operation Information

Basic Operation

The output of this single inverter buffer/driver is open drain, and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered. The Ioff feature also allows for live insertion.

Function Block Diagram



Feature Description

- Wide operating Vcc range of 0.8V to 3.6V.
- 3.6-V I/O tolerant to support down translation.
- Input hysteresis allows slow input transition and better switching noise immunity at the input.
- Ioff feature allows voltages on the inputs and outputs when Vcc is 0 V.
- Low noise due to slower edge rates.

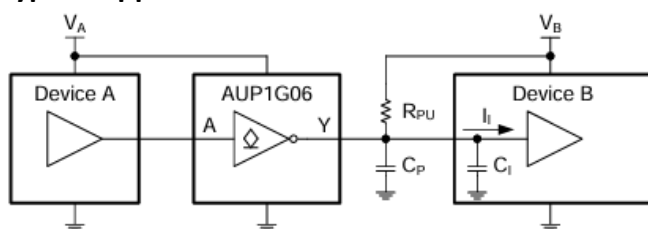
Device Functional Table

INPUT A	OUTPUT Y
L	Hi-Z
H	L

IC Application Information

Open-drain devices are very commonly used for voltage level translation. In this application, the CL74AUP1G06 is used to translate a 1.8-V output from device A to a 3.3-V input on device B

Typical Application



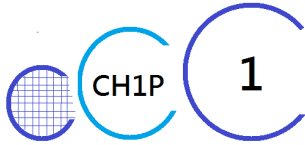
Design Requirements

This device has a standard CMOS input, so be careful to avoid slow or floating inputs that might cause oscillation or excessive current.

This device has an open-drain output, which means that the output enters a high-impedance state when a normal CMOS device would drive the output high. A pull-up resistor must be added to the output for an open drain device to have a high output. The selection of this pull-up resistor is detailed in the next section

Detailed Design Procedure

1. Recommended Input Conditions
 - For specified high and low levels, see VIH and VIL in the Electrical Characteristics table.
 - Inputs are overvoltage tolerant allowing them to go as high as VI(max) in the Absolute Maximum Ratings table at any valid VCC.
2. Recommended Output Conditions
 - Output voltage must not exceed VO(max) as specified in the Absolute Maximum Ratings table.
 - Pull-up resistor (R) selection depends on three primary factors: desired output high voltage (VOH), which is directly related to total leakage current into the CL74AUP1G240 and the peripheral device's input (IL), desired 0 to 90% rising edge time (tr), which is directly related to the parasitic line capacitance (CP), and the maximum current during low output (IOL), which is directly related to the supply value. These three equations govern pull-up resistor selection
 - $R \leq (V_{CC} - V_{OH}) / I_L$
 - $R \leq tr / (2.3 * C_P)$
 - $R \geq V_{CC} / I_{OL(max)}$

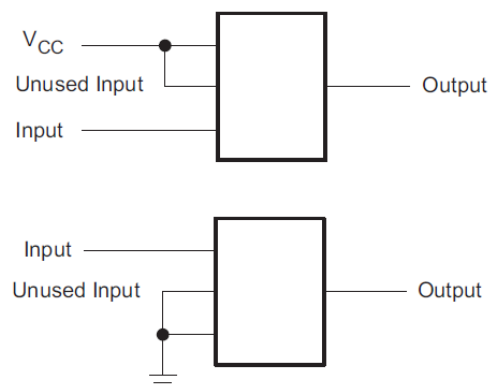


Power Supply Recommendations

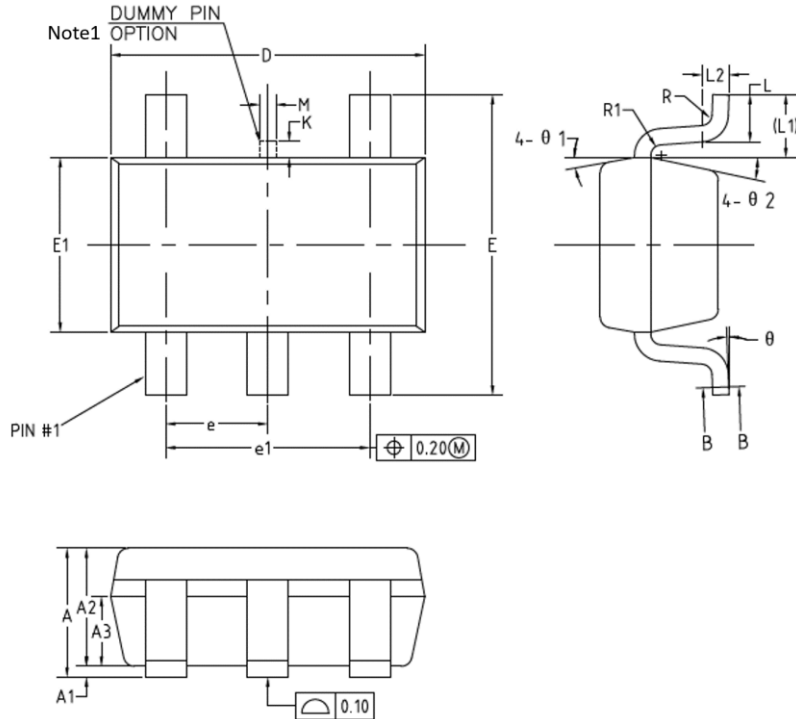
The power supply can be any voltage between the Min and Max supply voltage rating located in the Recommended Operating Conditions table. Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended; if there are multiple VCC pins, then 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and a 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

Layout Considerations

When using multiple-bit logic devices, inputs should never float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Below figure specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.



Package Information SOT23-5



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.25
A1	0	—	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
△ b	0.34	—	0.45
△ b1	0.34	0.38	0.41
△ c	0.12	—	0.20
△ c1	0.12	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
△ E1	1.526	1.626	1.700
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
△ K	0	—	0.20
L	0.30	0.40	0.60
L1	0.59REF		
L2	0.25BSC		
△ M	0.10	0.15	0.20
R	0.05	—	0.20
R1	0.05	—	0.20
θ	0°	—	8°
θ 1	8°	10°	12°
θ 2	10°	12°	14°

Notes: 1. Dummy pin may differ or may not be present.

